

2FHD0220

Application Manual

SiC MOSFET Plug-and-Play Driver

The 2FHD0220 is a plug-and-play dual-channel SiC gate driver developed by Firstack for 62mm housing module with the blocking voltage up to 2000V.

The 2FHD0220 integrates comprehensive protection, intelligent fault management and configurable gate voltage. It supports differential signal inputs and has a compact design for applications requiring high power density and signal quality.

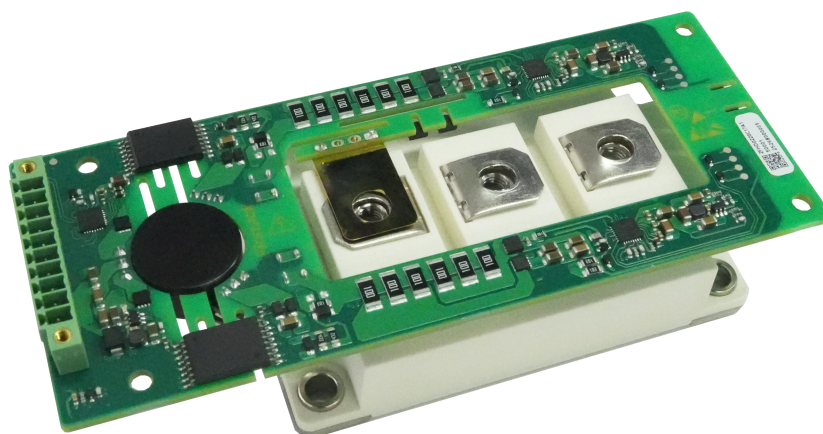


Fig.1 2FHD0220

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Abstract

2FHD0220 is a high-performance, plug-and-play dual-channel gate driver developed by Firstack based on our ASIC platform. It adopts capacitive coupling isolation. The primary side is equipped with 1x10 input interface, the default input signal is differential signal, can support single-ended signal. The overall architecture is shown in Fig. 2:

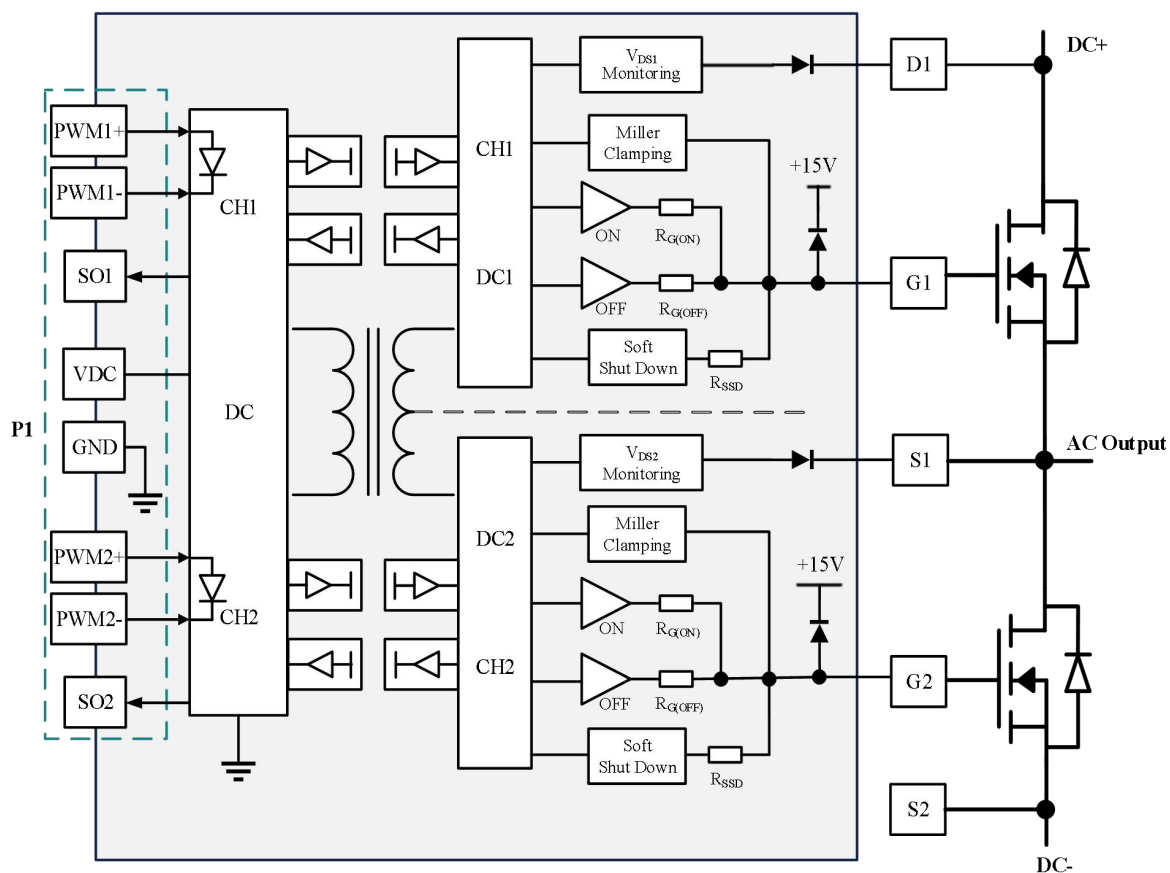


Fig. 2 2FHD0220 block diagram

How to assemble

A soft copper sheet is used on the 2FHD0220 to connect the module drain (D). During installation, the copper sheet must be placed on the surface of the module's power terminals and then tightened with screws. The copper sheet connects to the high voltage side of the module, so the customer's busbar design needs to allow for a safe distance to prevent any accidental contact.

NTC Notification

2FHD0220 does not provide NTC sampling function, the module temperature information sampling needs to be led to the control board by the customer.

Change the Input PWM Signal

The 2FHD0220 provides two types of signal inputs: single-ended and differential. When using differential signal input, pins 4 and 6 do not require any processing. When using single-ended signals, pins 4 and 6 need to be grounded. Customers can choose their pin definitions according to the actual situation. If you are using a bullhorn terminal, a terminal shift board will be included with the purchase of the 2FHD0220 for the convenience of the customer, and the pin definitions of the bullhorn terminals are as follows:

NC	1	2	GND
NC	3	4	GND
VDC	5	6	GND
VDC	7	8	GND
SO1	9	10	GND
PWM1+	11	12	PWM1-
SO2	13	14	GND
PWM2+	15	16	PWM2-
NC	17	18	GND
NC	19	20	GND

Use steps and safety notice

Simple use steps of the gate driver are as follows:

1. Choose suitable gate driver

When using the gate driver, pay attention to the model of the SiC module that the gate driver is adapted to. It is invalid for non-designated SiC modules. Improper use may cause the gate driver and the module failure.

2. Install the gate driver on the SiC module

Any treatment of SiC modules or gate drivers should follow the general specifications for the protection of electrostatic sensitive devices required by the international standard IEC 60747-1, Chapter IX or IEC 60340-5-2 (which means the workplace, tools, etc. must comply with these standards).

If these specifications are ignored, both the SiC module and the gate driver may be damaged.



3. Connect the gate driver to the control unit

Connect the gate driver connector to the control unit and input a suitable supply voltage to the gate driver.

4. Check the function of the gate driver

Check the gate voltage: for the turn-off state, the rated gate voltage is given in the corresponding data sheet. At this time moment the turn-on voltage will be different according to the modules. Please also check the input current of the gate driver with and without a control signal.

These tests should be performed before installation, because the gate terminal may not be accessible after installation.

5. Set up and test the power unit

Before starting the system, it is recommended to check each SiC module with a single pulse or double pulse test method. Firstack specially reminds: even under the worst conditions, it is

necessary to ensure that the SiC module does not exceed the operating range specified by SOA, because the operating condition of the SiC module strongly depends on the specific converter architecture.

Primary Side Characteristics

Description of primary side interface

VDC	1
GND	2
PWM1+	3
PWM1-	4
PWM2+	5
PWM2-	6
SO1	7
SO2	8
GND	9
GND	10

2FHD0220 use a 1x10 terminal in primary side.

- 1x power supply V_{DC}
- 3x GND
- 1x PWM1+
- 1x PWM1-
- 1x PWM2+
- 1x PWM2-
- SO1
- SO2

(1) V_{DC}

The 2FHD0220 is equipped a VIN power terminals, which supplies the power to both primary side and isolated DC/DC converter, in order to provide positive and negative voltage to secondary side. Without load, the maximum required current of the gate driver is 180mA.

(2) PWM_x +/-

The default input signal of the 2FHD0220 is a differential signal input, so it is necessary to use two signal wires. PWM - can be grounded to be compatible with single-ended signal use as required. The positive and negative difference of the input differential signal is 15V.

(3) SOx

The status output pins can output fault signals for the top and bottom switches respectively. 2FHD0220 defaults to a supply voltage of 15V using a 10kΩ resistor pull-up.

Technical Principle

1. Power Supply and Electrical Isolation

The gate driver implements isolated power and signal. Power isolation is realized by the transformer, signal isolation is realized by optical interface. The transformer complies with the safety isolation standard EN50178 and the primary and secondary sides fulfil protection class 2.

Please note that a stable supply voltage and current are required to power the driver.

2. Power Monitoring

The primary side of the driver and the two secondary side power supplies have local power detection circuits and corresponding undervoltage lockout.

When undervoltage occurs in the primary side power supply, both SiCs are driven by the negative gate voltage to maintain the shutdown state (both channels are blocked), and SO1 and SO2 both feed back the fault status signal to the host computer.

When the positive or negative voltage on the secondary side is lower than the threshold voltage, the driver circuit will determine that an undervoltage fault has occurred, and the driver circuit will automatically block the SiCs, while the corresponding SOx feeds back a fault signal to the host computer.

The SOx outputs will automatically reset after the primary and secondary undervoltage faults are eliminated.

Firstack recommends not to let any of the SiCs in the bridge arm operate in an undervoltage state.

3. Operating Mode

Direct Mode:

IN1 and IN2 are independent signals. CH1 and CH2 can be turned on simultaneously.

Half-Bridge Mode:

PWM1 is the drive signal input (PWM), PWM2 is the input enable terminal (EN);

PWM2 is low, the two output channels are blocked, and no action is taken regardless of whether PWM1 is driven by a signal.

PWM2 is high, the two output channels are enabled and the output signal follows the input signal PWM1.

When PWM2 is high, PWM1 changes from low to high, the CH2 gate signal is blocked immediately, and after a dead time T_d , the CH1 gate is turned on. Fig. 3 shows the specific signal logic.

Note: The 2FHD0220 is in direct mode by default, if configured in half-bridge mode, the dead time T_d is set by software and cannot be changed externally. when PWM1 goes from low to high, it needs to go through a dead time before the output follows the change of PWM2.

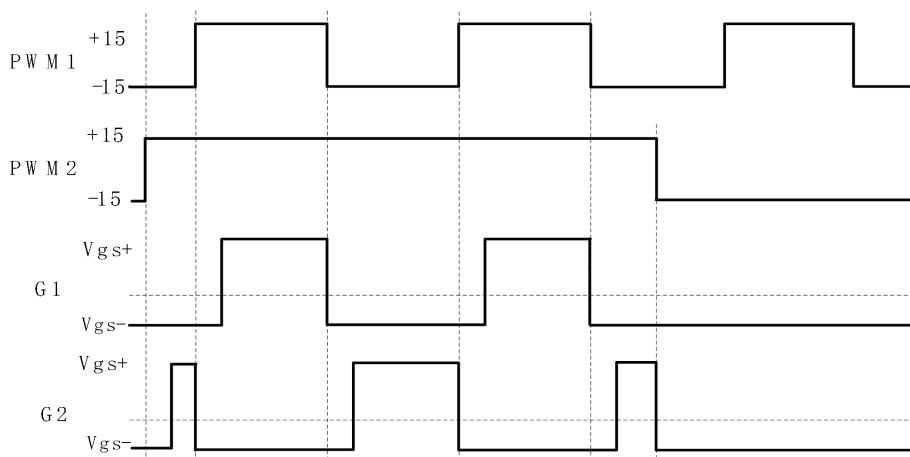


Fig. 3 Half-Bridge mode logic

When performing a double-pulse test, testing the bottom switch (PWM2) simply sends the wave normally. When testing the top switch (PWM1), you need to keep the bottom switch high and then send a PWM signal to the top switch.

2. Intelligent Fault Management

The driver detects the operation status of the module in real time, and when the module fails, it uploads the fault status to the host computer through the SOx output, and the 2FHD0220 realizes the fault differentiation by the difference of the pull-down time of the SOx signal (the time of the fault return).

See the following table for specific information on differentiation:

Fault Types	Short Circuit	Sec. UVLO	Pri. UVLO	Other Faults
Return Time (Tsox)	10ms	20ms	40ms	80ms

4. SC Protection and Soft Shut Down

The 2FHD0220 is capable of detecting short circuits during SiC module operation and initiating soft shutdown to safely shut down the module. Currently, the mainstream short-circuit protection detection is through desaturation detection, of

which there are two detection methods: resistance detection and diode detection. 2FHD0220 uses the diode detection function, the functional schematic diagram is shown in Fig. 7.

The diode detection circuit can realize high precision and fast response to protect the module in short-circuit condition.

The signal logic is shown in Fig. 5. During normal operation, current will flow through a low impedance circuit consisting of a diode and a resistor to limit the current. When a short circuit occurs, V_{DS} will rise due to module desaturation, causing the diode to reverse cutoff so that current will no longer flow through the diode and begin charging capacitor C1. After a charging time t_{RC} voltage exceeds the threshold V_{ref} (set by the SW), and after a filtering time t_{DS_FLT} (set by SW), the TC signal is activated, and the SSD signal will switch from low to high to start the soft turn-off. In order to prevent the short-circuit protection function from being triggered by mistake when V_{DS} falls at the turn-on time, a certain SCS time t_{BL} (short-circuit protection blocking time, set by SW) needs to be set.

When a short circuit is detected, the gate signal will be in a high impedance state, the SSD signal will be set high, Q3 will be turned on, and the current will flow through the SSD resistor R3 to realize soft turn-off, thus effectively suppressing the turn-off spikes brought about by high di/dt .

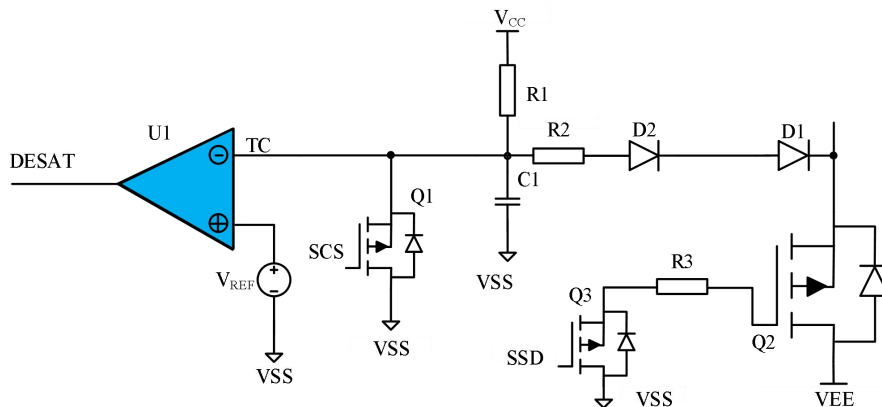


Fig. 4 SC detection circuit

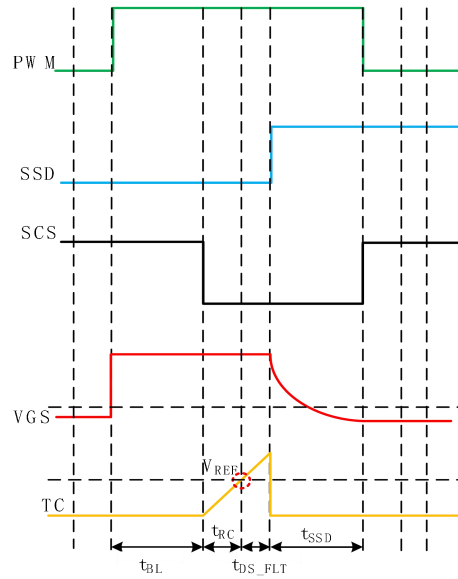


Fig. 5 SC protection and SSD time sequence diagram

5. Active Miller Clamping (AMC)

The AMC pulls the gate voltage down to a certain negative voltage, which is used to suppress the half-bridge crosstalk caused by SiC at high dv/dt . The positive overshoot will cause a short circuit of the gate conduction, and the negative overshoot will cause damage to the gate. The gate miller clamping design schematic is shown in Fig. 5.

Fig. 6 illustrates the active miller clamping signal logic. During turn-on, the AMC signal is low; during turn-off, after a filtering time of t_{AMC_ON} , the AMC signal will be converted to a high level to initiate the miller clamping. The time of t_{AMC_ON} can be configured by software, the default time of 2FHD0220 is 1.04us, and t_{AMC_OFF} is a fixed time of 300ns.

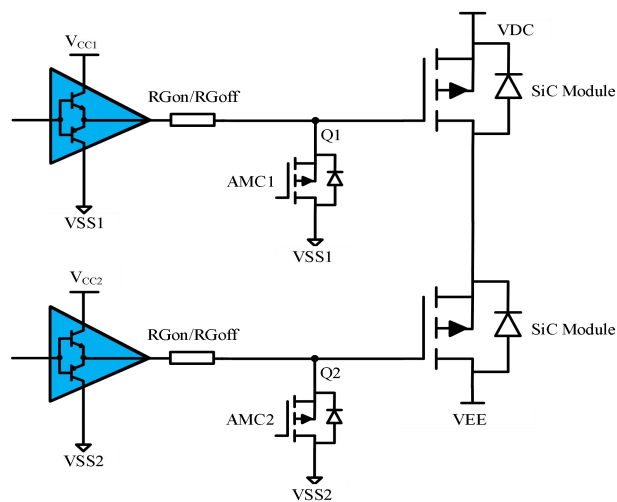


Fig. 5 AMC Circuit

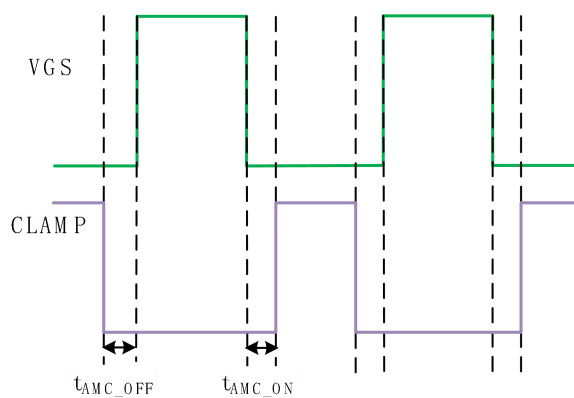


Fig. 6 AMC Signal Logic

Update History

Date	Description	Version
2025.07.24	Official Version	V1.0

Technical Support

Firststack's professional team will provide you with business consultation, technical support, product selection, price, lead time and other related information, and guarantee to answer your questions within 48 hours.

Legal Disclaimer

The instruction manual provides a detailed description of the product but does not commit to providing specific parameters regarding the delivery, performance, or applicability of the product. This document does not offer any express or implied warranties or guarantees.

Firststack reserves the right to modify technical data and product specifications at any time without prior notice. The general delivery terms and conditions of Firststack apply.

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