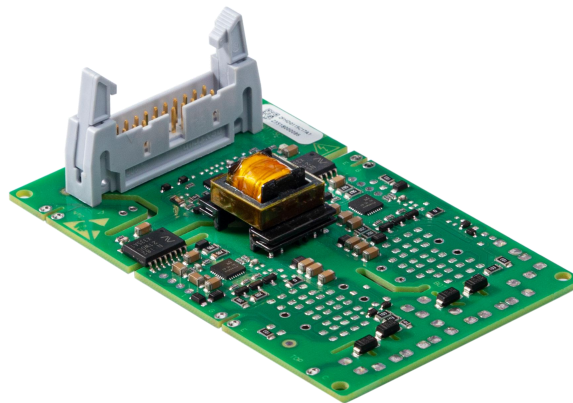# 2FHD0115C

Application Manual

Electrical interface gate driver solution for EconoDUAL modules, support multi-level

The 2FHD0115C is a dual-channel gate driver with electrical interface and ASIC digital control, which can safely and reliably drive the IGBT. The 2FHD0115C is suitable for Infineon EconoDUAL as well as other brands of IGBTs in the same package. The plug-and-play gate driver can be assembled directly without secondary development.
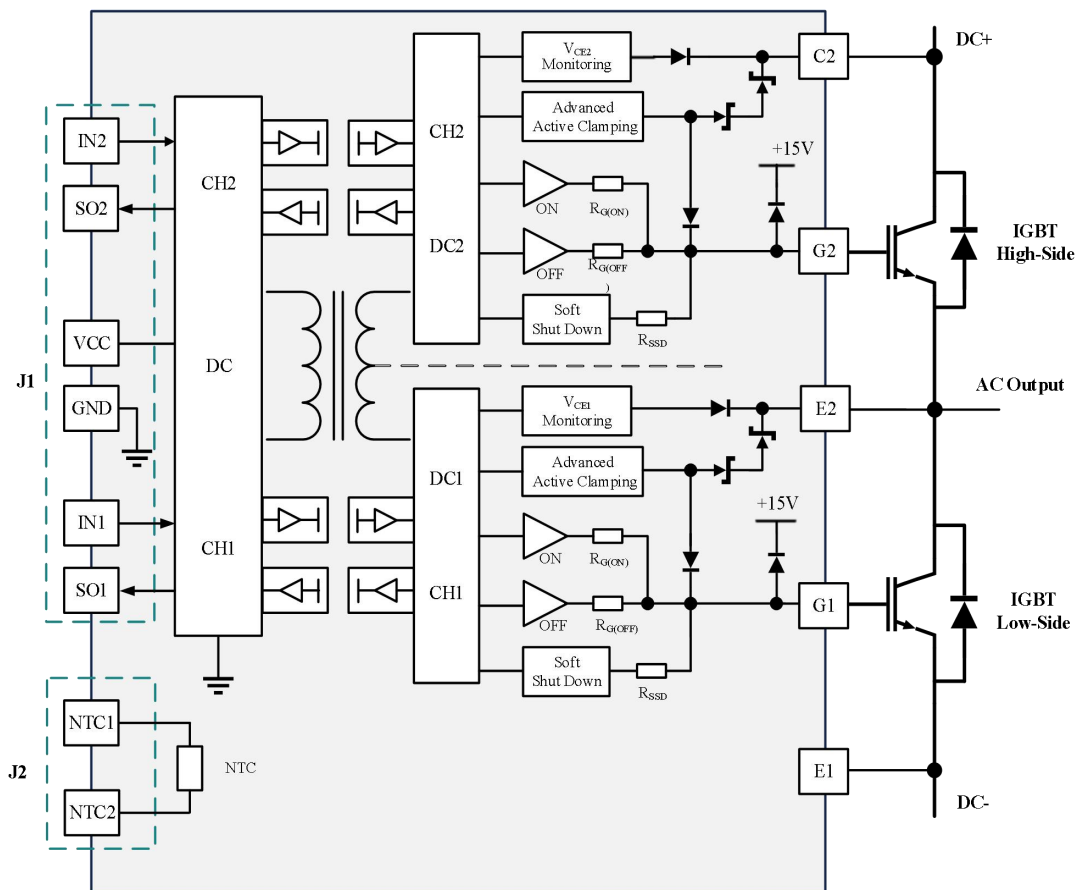

Fig.1　2FHD0115C

Contents

Driver Overview

The 2FHD0115 is a plug-and-play gate driver developed by Firstack based on digital control. The basic block diagram is shown in **Fig.2**, and the values of the gate resistors and other key components can be found in the data sheet of the corresponding gate driver.

Fig.2   2FHD0115 block diagram

The gate driver has built-in input connector J1, isolated DCDC power supply, driving circuit with Vce sense (short-circuit protection), undervoltage protection, active clamping, soft shut down, Miller clamp (reserved), etc., which can safely and reliably drive IGBT modules.

Use Steps and Safety Notice

Simple use steps of the gate driver are as follows:

1. Choose suitable gate driver

When using the gate driver, pay attention to the part number of the IGBT module that the gate driver is adapted to. It is invalid for non-designated IGBT modules. Improper use may cause the drive and the module failure.

2. Install the gate driver on the IGBT module

Any treatment of IGBT modules or gate drivers should follow the general specifications for the protection of electrostatic sensitive devices required by the international standard IEC 60747-1, Chapter IX or IEC60340-5-2 (which means the workplace, tools, etc. must comply with these standards).

If these specifications are ignored, both the IGBT and the gate driver may be damaged.

3. Connect the gate driver to the control unit

Connect the gate driver connector to the control unit and provide a suitable power supply voltage for the gate driver.

4. Check the function of the gate driver

Check the gate voltage: for the off state, the rated gate voltage is given in the corresponding data sheet; for the on state, the voltage is 15V. Please also check the input current of the gate driver with and without a control signal.

These tests should be performed before installation, because the gate terminal may not be accessible after installation.

5. Set up and test the power unit

Before starting the system, it is recommended to check each IGBT module with single pulse and double pulse test method separately. In particular, Firstack recommends that users ensure that the IGBT module does not exceed the operating range specified by SOA even under the worst conditions, as this is strongly dependent on the specific converter architecture.

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Even when testing a single IGBT, power must be supplied to the remaining gate drivers in the system to ensure that the gates of all other IGBTs operate in negative voltage off state. This is particularly important when testing the switching behaviour of an IGBT.

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2FHD0115 Recommended Application Circuitry
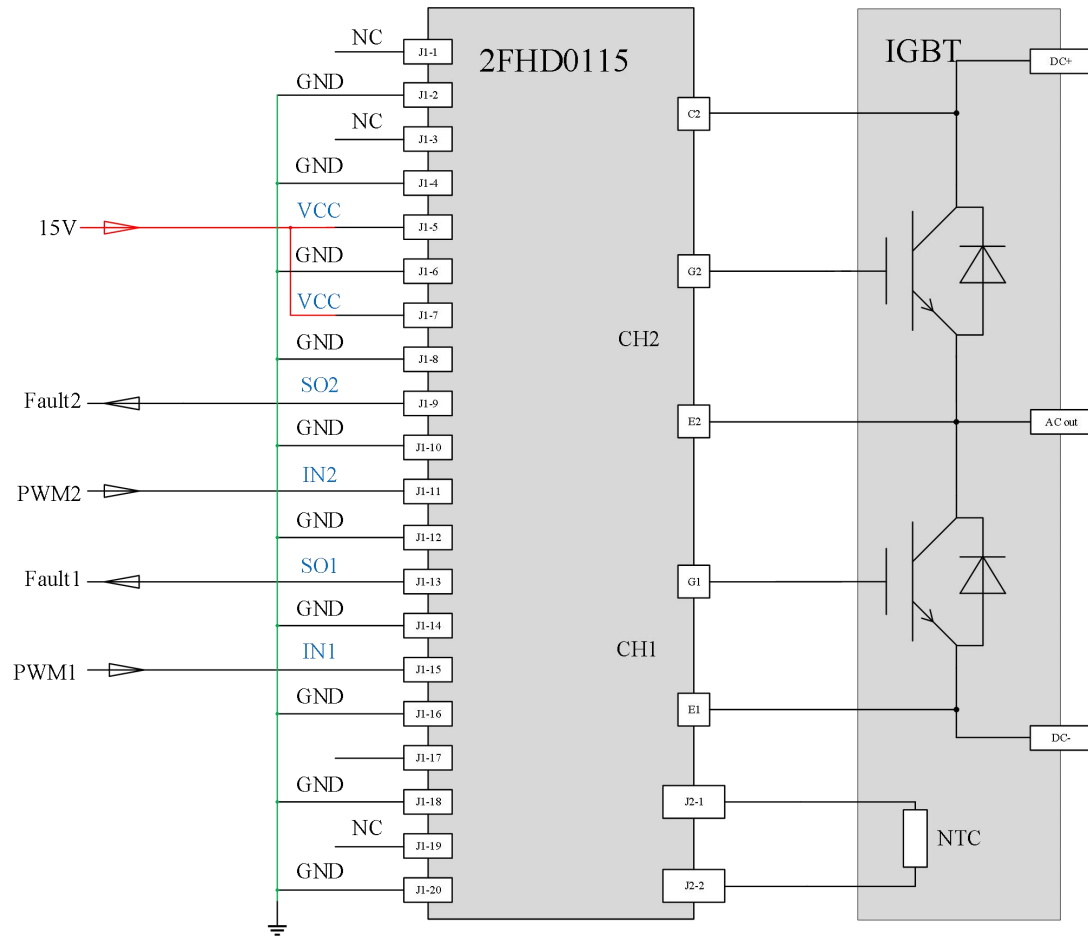
Fig.4 Recommended user interface of 2FHD0115

J1 connector pin designation

Pin	Designation	Function	Pin	Designation	Function
1	NC	Free	2	GND	Primary side ground
3	NC	Free	4	GND	Primary side ground
5	VCC	Power supply input	6	GND	Primary side ground
7	VCC	Power supply input	8	GND	Primary side ground
9	SO2	Top IGBT status output	10	GND	Primary side ground
11	IN2	Top IGBT signal input	12	GND	Primary side ground
13	SO1	Bottom IGBT status output	14	GND	Primary side ground
15	IN1	Bottom IGBT signal input	16	GND	Primary side ground
17	NC	Free	18	GND	Primary side ground
19	NC	Free	20	GND	Primary side ground

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Description of Connector J1 Interface

Abstract

The J1 interface circuitry of 2FHD0115 gate driver is quite simple and easy to use.

The J1 connector is equipped with the following terminals:

- 2x power-supply terminals (only one 15V supply is required)

- 2x driving signal inputs

- 2x fault signal outputs

- 10x GND (ground)

- 4x NC (free)

The gate driver comes with a 20-pin interface connector with all even pins configured as GND and odd pins configured as inputs or status outputs. The 20-pin twisted flat cable is recommended. Each input and output signal line is then twisted with its GND line. All GND pins are connected together on the 2FHD0115 and should be connected to the control board side, which reduces parasitic inductance while increasing immunity.

VCC

There are two VCC power terminals on the J1 connector for primary side circuitry and isolated DCDC power.

The total power of the driver is 2*1.5W+1.5=4.5W, and at 80% efficiency, 15V requires an input current of 375mA, which limits the start-up impulse current.

INx

The gate driver input signal pin, support 5~15V logic level, the function of INx is related to the mode set by the gate driver, the software can set the mode of the gate driver, the hardware cannot. Ax and Bx are the direct mode, Dx is the half-bridge mode. Please select the corresponding gate driver part number according to the driving signal mode of the main control board.

Direct mode:

IN1 and IN2 are independent of each other and are both signal inputs for the corresponding channel, channel 1 and channel 2 can be turned on at the same time.

In half-bridge applications, it is necessary to ensure that there is sufficient dead time between IN1 and IN2.

Half-bridge mode:

In this mode, IN1 is the driving signal input (PWM), and IN2 is the signal input enable terminal (EN); if IN2 is low, the output signals of both channels are blocked, if IN2 changes from low to high, the two output channels are enabled and the output signals follow the input signal (PWM). In half-bridge mode, channel 1 and channel 2 will not turn on at the same time, the default setting of dead time is 4us, software can be customized.

The half-bridge mode logic is shown below:
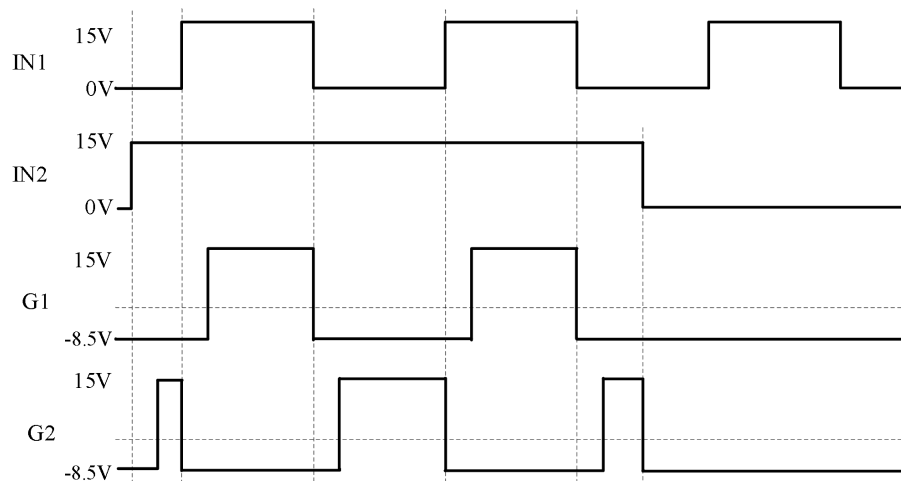
Fig.5 The half-bridge mode logic

SOx

The output SOx is in the form of an open-drain transistor and defaults to a separate fault signal in order to pinpoint the problem. They can also be connected together to provide a common fault signal.

The value of the current flowing through the SOx under fault condition must not exceed the maximum value specified in the data sheet.

SOx is open-drain mode (OD)

When there is no fault detected, the output is in high resistance state, it is necessary to connect the pull-up resistor externally, and the pull-up voltage range is recommended to be 5~15V.

When a fault is detected on channel 'x', the status output SOx terminal is pulled low (connected to GND).

SOx is pull-up mode

When the fault is not detected, the output is 15V. The gate driver is internally pulled up by a 10K resistor, so when the external SOx external resistor is connected, attention needs to be paid to impedance matching to avoid system misjudgment due to voltage division.

When a fault is detected on channel 'x', the status output SOx terminal is pulled low (connected to GND).

SOx output logic

When an undervoltage occurs on the primary side of the gate driver, the gate performs negative turn-off directly and maintains the blocking signal for one blocking time while both SOx report a 40ms low level fault once and then return to high level for 40ms.

If the undervoltage disappears before the end of the above process, SOx will remain high; if the undervoltage still exists at the end of the above process, the fault will be pulled low again until the fault disappears, and then flips to high after one blocking time (80ms).

Primary side blocking signal: after the undervoltage on the primary side disappears, the blocking ends after another 80ms and the primary side processes the INx signal normally.

When an undervoltage occurs on the secondary side of the gate driver, the gate first performs soft shut down, then puts in a negative voltage for a certain period of time, after which it maintains 0V shutdown and maintains blocking signal, and the corresponding SOx signal reports a 20ms low level fault and then returns high for 100ms.

If the secondary side undervoltage disappears before the end of the above process, SOx remains high; if the secondary side undervoltage still exists at the end of the above process, the fault signal is pulled low again until the fault disappears, and after another 80ms, the SOx signal flips to high.

Primary side blocking waveform: after the undervoltage on the secondary side disappears, the blocking ends after 60~80ms, and the primary side processes the INx signal normally.

When a short-circuit occurs on the secondary side of the gate driver, the gate first performs the soft shut down, then puts in negative voltage to keep the shutdown state and maintains the blocking signal, the corresponding SOx signal reports the fault, and then automatically returns high after pulling down for 10ms.

Description of Connector J2 Interface

NTC Terminal

The gate driver uses a non-isolated IGBT module NTC output on interface J2, which is directly connected to the NTC thermistor of the IGBT module, and the gate driver does not isolate this signal. **This terminal is not installed by default.**

Technical Principle

Function Description

The 2FHD0115 series plug-and-play drivers are used in EconoDUAL equivalently packaged IGBT modules.

Basic functions: signal isolation, DCDC power isolation

Protection functions: short-circuit protection, undervoltage protection, soft shut down, active clamping, fault blocking signal, status feedback

Digital functions: intelligent fault management

The gate drivers support direct connection in parallel, as well as multi-level applications.

Power Supply and Electrical Isolation

This gate driver implements isolated power and signal. Power isolation is realized by the transformer, signal isolation is realized by capacitive coupling. The transformer complies with the safety isolation standard EN50178 and the primary and secondary sides fulfil protection class 2. Please note that a stable supply voltage and current are required to the gate driver.

Power-Supply Monitoring

The primary side of the gate driver, as well as the two secondary side power supplies, have local power sense circuits and corresponding undervoltage protection.

When an undervoltage occurs at the power supply of the primary side, both IGBTs are driven by the negative gate voltage to maintain the turn-off state (both channels are blocked), both SO1 and

SO2 feed back the fault status signal to the master computer.

When the positive or negative voltage of the secondary side is lower than the threshold voltage, the driving circuit will determine that an undervoltage has occurred, and automatically block the IGBT. At the same time, the corresponding SOx feeds back a fault signal to the master computer.

The SOx outputs are automatically reset after the primary and secondary side undervoltage removed.

The SOx outputs are automatically reset after the primary and secondary side undervoltage removed and the corresponding fault return time (refer to Intelligent Fault Management).

Firstack recommends that any IGBT in the bridge arm should not operate in an undervoltage state.

1. Due to the presence of C_{CG}, when one IGBT in the bridge arm turns on, the high dv/dt from it can be coupled to the other IGBT through the C_{CG}, resulting in micro-conduction of the other IGBT.

2. Undervoltage on the primary and secondary side results in a lower gate voltage, which in turn causes an increase in IGBT switching losses.

Short-circuit Protection

The driving circuit judges whether the IGBT is in a short-circuit state by detecting the collector voltage V_{CE} when the IGBT is turned on.

The V_{CE} voltage is detected by high-voltage diode. When the V_{CE} voltage exceeds the set threshold, the gate driver determines that the IGBT is in a short-circuit state, starts the soft shut down to slowly turn the IGBT off, and returns the fault to the master computer at the same time.
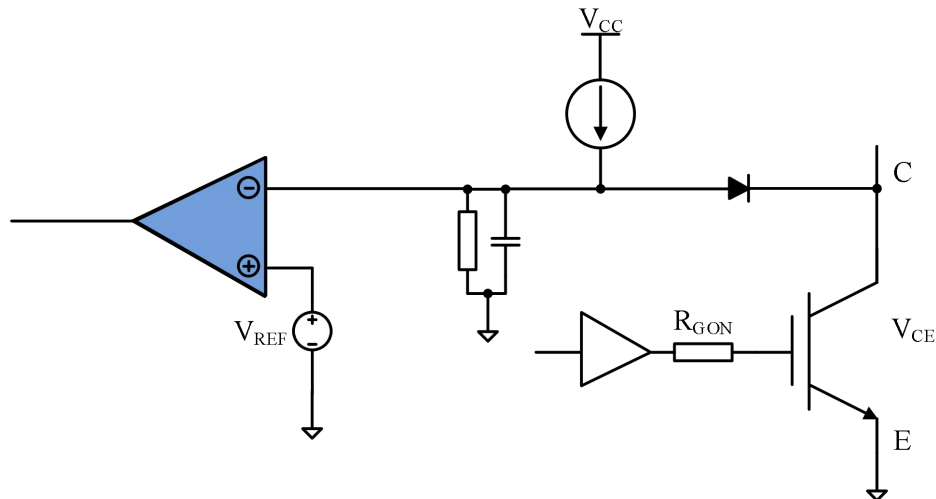
Fig.6　V_{CE} desaturation sense circuit

The V_{CE} is detected after a response time in the on-state (refer to **Fig.6**) to determine the short-circuit condition. If this voltage is higher than the preset threshold Vth, the gate driver determines that the IGBT has a short-circuit and sends a fault signal to the corresponding SOx output. At the same time, soft shut down is initiated to turn off the IGBT slowly. The IGBT keeps in the off-state (cut off), the pin SOx output fault state lasts for 10ms and then returns to high level, and the fault blocking time lasts for 80ms.

Note: the desaturation sense function is only used for short-circuit protection and cannot provide overcurrent protection.
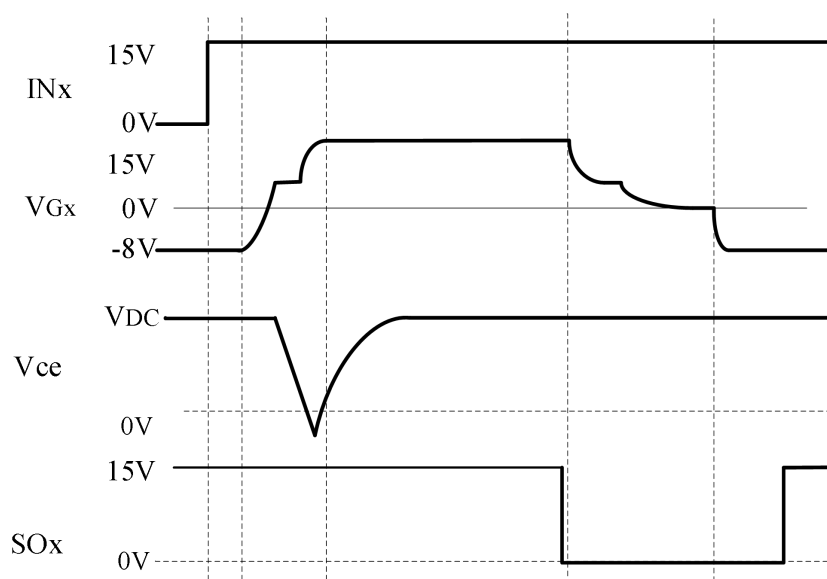
Soft Shut Down

When the IGBT desaturation occurs, V_{CE} reaches the bus voltage. At the same time, the I_C will reach 4 times of the rated current or even more and the di/dt at the turn-off time will form a very high voltage peak on the parasitic inductance, which will easily damage the IGBT.

When the IGBT desaturation is triggered, the digital core will detect and trigger soft shut down to turn off the IGBT. Within 10us, the IGBT is gradually turned off by slowly lowering the gate voltage Vge, which effectively reduces the di/dt, and then reduces the voltage peak at the turn-off moment. Thus, the short-circuit protection of IGBT is achieved.

Active Clamping

The active clamping function triggers the active clamping action when the collector-emitter voltage exceeds the preset threshold, which partially turns on the IGBT, thus suppressing the collector-emitter voltage of it, and the IGBT operates in the linear region.

The 2FHD0115C adopts six TVS to form a basic active clamping, which can effectively suppress the turn-off overvoltage peak.

For 1200V IGBT, 5pcs of SMBJ150A are recommend, plus 1pcs of SMBJ150CA.

For 1700V IGBT, 5pcs of SMBJ220A are recommend, plus 1pcs of SMBJ220CA.

All of the above applications use a bidirectional TVS (SMBJxxCA) to prevent current from flowing from the G to the C through the TVS loop.

Intelligent Fault Management

The gate driver detects the operation status of the module in real time, and when there is a fault, the module uploads the fault status to the master computer through the SOx output. The 2FHD0115 realizes the fault differentiation by the difference of the SOx signal pull-down time (fault return time).

For more information, please see the table below.

Fault type	SC	UVLO(sec.)	UVLO(pri.)	Other faults
Fault return time	10ms	20ms	40ms	80ms

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Technical Support

Firstack's professional team will provide you with business consultation, technical support, product selection, price, lead time and other related information, and guarantee to answer your questions within 48 hours.

Legal Disclaimer

The instruction manual provides a detailed description of the product but does not commit to providing specific parameters regarding the delivery, performance, or applicability of the product. This document does not offer any express or implied warranties or guarantees.

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