2FHD0620

Application Manual

SiC plug-and-play gate driver

The 2FHD0620 is a dual-channel SiC gate driver developed by Firstack for up to 1700V EconoDual module, which can be used as plug&play GDU(gate driver unit) or cooperated with A1EDB1V-S0002 for max. 4 modules in parallel.

The gate driver incorporates advanced features such as active Miller clamping, soft shut down and distributed NTC sampling, which can safely and reliably drive the SiC MOSFET module.

Fig.1 2FHD0620

Contents

Abstract

The 2FHD0620 is a high-performance, dual-channel gate driver developed based on intelligent chip technology by Firstack, supports SiC modules up to 1700V. The module control core (MCC) and main module adaptor board (M-MAB) are connected by pin headers, and can be used as plug-and-play drivers. With customized cables and sub adaptor boards (S-MAB), the gate driver can support up to 4 parallel connections, and the overall architecture is shown in **Fig.2**:

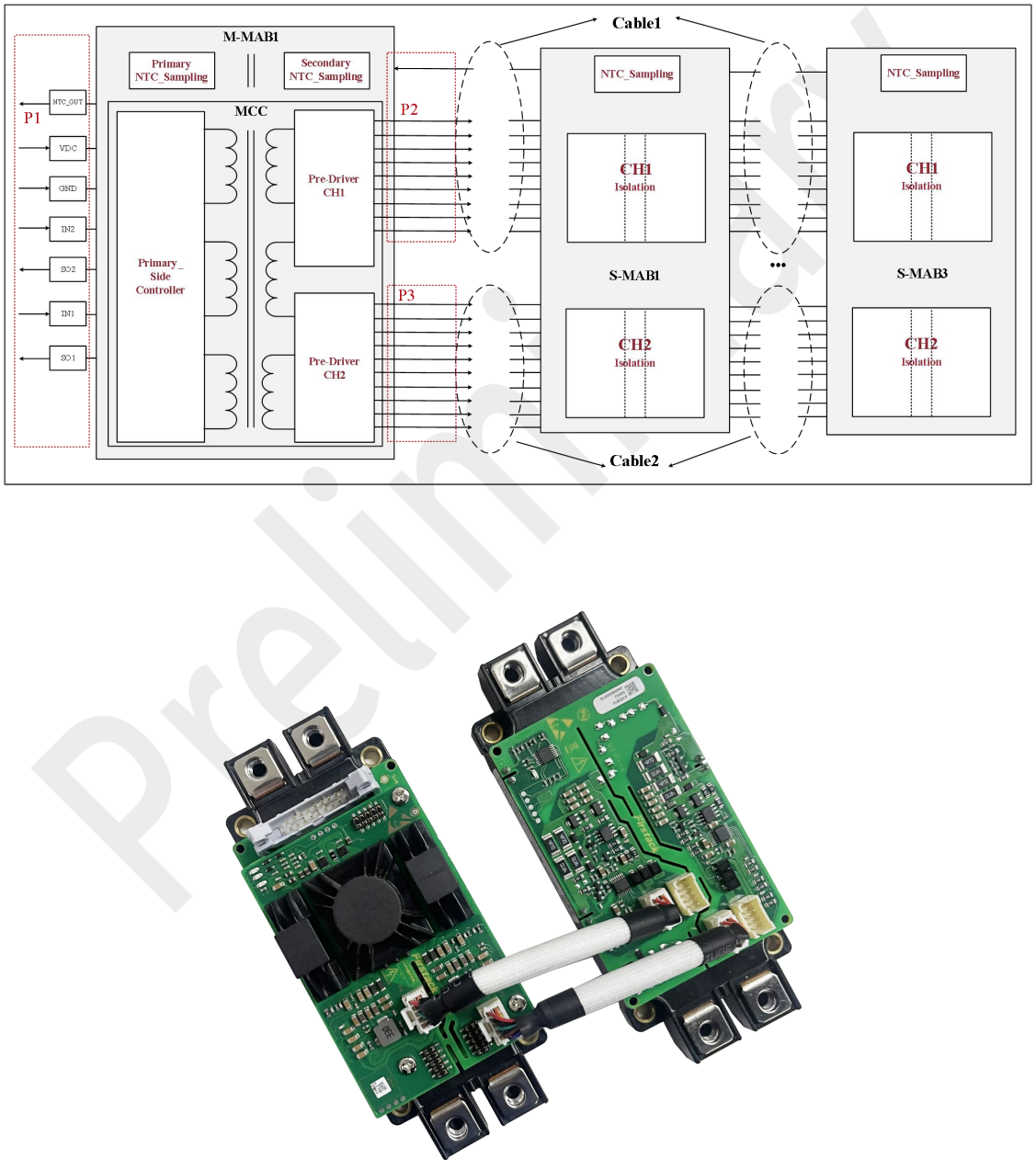


Fig.2 2FHD0620 block diagram

Use steps and safety notice

Simple use steps of the gate driver are as follows:

1. Choose suitable gate driver

When using the gate driver, pay attention to the model of the SiC module that the gate driver is adapted to. It is invalid for non-designated SiC modules. Improper use may cause the gate driver and the module failure.

2. Install the gate driver on the SiC module

Any treatment of SiC modules or gate drivers should follow the general specifications for the protection of electrostatic sensitive devices required by the international standard IEC 60747-1, Chapter IX or IEC 60340-5-2 (which means the workplace, tools, etc. must comply with these standards).

If these specifications are ignored, both the SiC module and the gate driver may be damaged.

3. Connect the gate driver to the control unit

Connect the gate driver connector to the control unit and input a suitable supply voltage to the gate driver.

4. Check the function of the gate driver

Check the gate voltage: for the turn-off state, the rated gate voltage is given in the corresponding data sheet. At this time moment the turn-on voltage will be different according to the modules. Please also check the input current of the gate driver with and without a control signal.

These tests should be performed before installation, because the gate terminal may not be accessible after installation.

5. Set up and test the power unit

Before starting the system, it is recommended to check each SiC module with a single pulse or

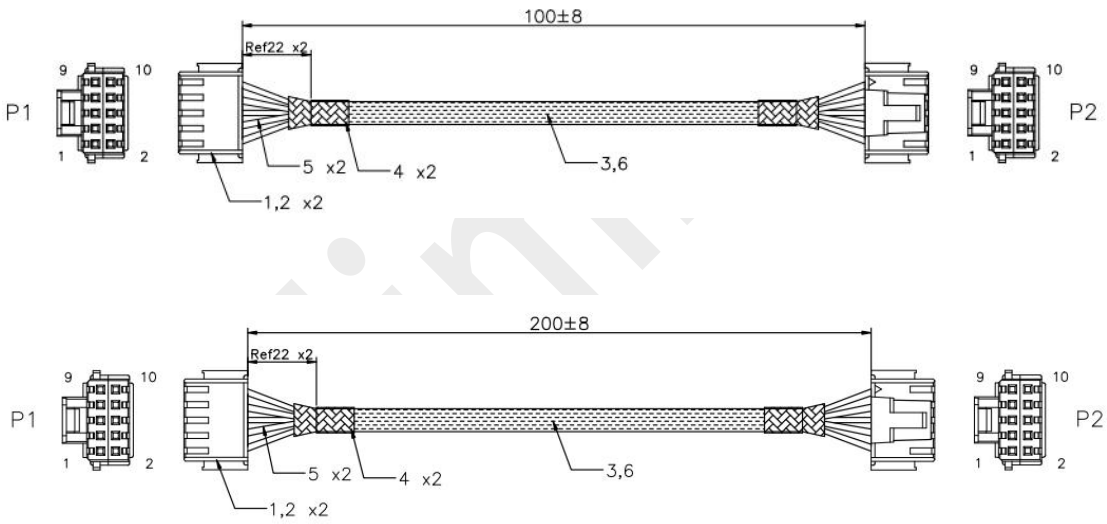
double pulse test method. Firstack specially reminds: even under the worst conditions, it is necessary to ensure that the SiC module does not exceed the operating range specified by SOA, because the operating condition of the SiC module strongly depends on the specific converter architecture.

Cable Description

With a set of cables 2FHD0620 is enable to be used for paralleling. There is prepared connectors for cables on the core board. Customer only needs to choose the suitable length of cable by actual application.

Note: The cable is special designed for corresponded product, if customer uses their own cables, Firstack can not promise the performance.

Cable Part Number	Cable Length (mm)	Pin Definition
JWDET-00618	200	3rd pin as ground
JWDET-00810	100	



Assemble/Disassemble Description

Three M3 screws are used to mount the core board and adaptor board in order to increase the flexibility of the GDU. By removing three M3 screws the core board can be easily disassembled.

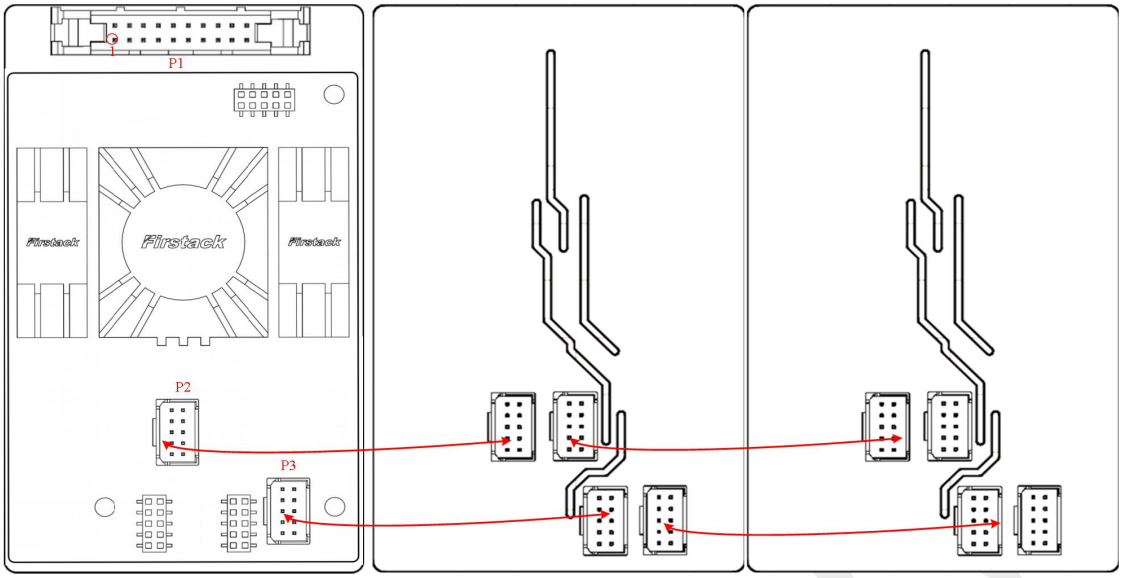
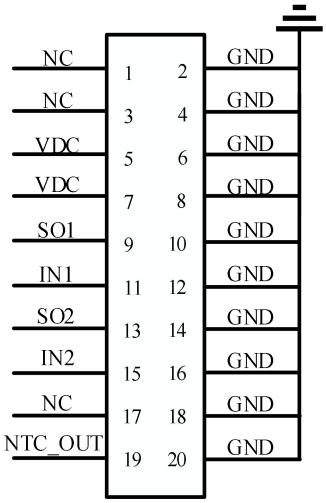


Fig.3 2FHD0620 cable connection guideline

Primary Side Characteristics

1. Description of Primary Side Interface



The primary side interface of 2FHD0620 is a 20-pin interface connector on the adaptor board:

- 2x power supply terminals V_{DC}
- 2x drive signal inputs INx
- 2x fault signal outputs SOx
- 10x GND (common ground)
- 1x NTC_OUT
- 3x NC (free)

2. V_{DC}

The 2FHD0620 is equipped two V_{DC} terminals, which supply the power to both primary side and isolated DC/DC converter, in order to provide positive and negative voltage to secondary side. The maximum current of the gate driver is 120mA.

3. INx

The signal input pins of the gate driver, support 5-15V logic level, the default setting is 15V output. The function of INx is related to the driving mode, which is selected by software(SW), and cannot be adjusted by hardware(HW).

Direct Mode:

IN1 and IN2 are independent signals. CH1 and CH2 can be turned on simultaneously.

Half-bridge topology: to avoid CH1 and CH2 both in high level, which causes the shoot-through due to the top and bottom bridge arm conduct at the same time, the dead time must be enough set by the control circuit.

Half-bridge Mode:

IN1 is the input terminal of drive signal (PWM), IN2 is the enable terminal (EN);

IN2 is low level, two outputs are blocked, all output signals are low level.

IN2 is high level, two outputs are enabled, output signals are changed follow the changing of IN1.

When IN2 is high level, IN1 converts from high to low level, the gate signal of CH2 is blocked immediately and turns on after dead time T_d.

Attention: The default mode of 2FHD0620 is direct mode. By using half-bridge mode the dead time T_d can be adjusted by SW, inaccessible by external sources. After a dead time during the process of IN2 from low to high, the output can follow the changing of IN1.

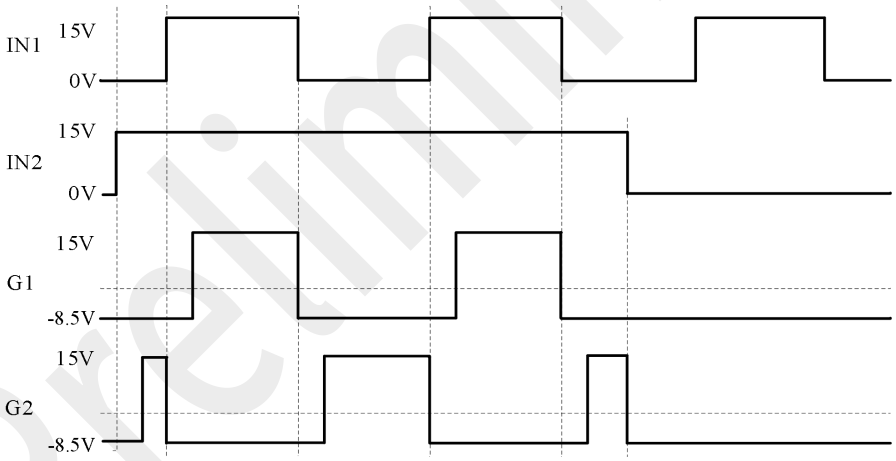


Fig.4 Logic diagram of half-bridge mode

4. SO1, SO2 Status Output

The outputs SOx have open-drain transistors, which is by default a single fault signal to locate the failure precisely. They can also be connected together to provide common fault signal. The 2FHD0620 pulls up to 15V fault output by default.

When channel “x” detects fault, SOx will be low (connected to GND).

SOx Output Logic

When an undervoltage occurs in primary side, the GDU will be negatively turned off directly and keep blocking for a blocking time, at the same time both of SOx goes to high after report 40ms low level fault.

If the undervoltage disappears before above process, SOx will keep high. If the undervoltage still occurs, the fault will be pulled down again until the fault disappears, then return to high after a blocking time (80ms).

Primary side blocking signal: After the primary side undervoltage fault disappears, after another 80ms the blocking is over, primary side process the INx signal normally.

When an undervoltage occurs in secondary side of the gate driver, gate performs soft shut down first. After the off status in negative voltage for a defined time, the signal will be blocked in 0V, the corresponding SOx signal reports 20ms low level fault and after that returns to high level 100ms.

If the undervoltage disappears before the above process, SOx keep high; If the fault still occurs, the signal will be pulled down again until the fault disappears, then after another 80ms the SOx signal returns to high level.

Primary side blocking signal: After the secondary side undervoltage fault disappears, then after 60-80ms the blocking is over, primary side process the INx signal normally.

When a short-circuit fault occurs on the secondary side of the driver, the gate first performs the soft shutdown function, then puts in a negative voltage to keep the shutdown state and maintains blocking signal, the corresponding SOx signal reports the fault, and then automatically restores the high level after pulling it down for 10ms.

The 2FHD0620 is equipped with Intelligent Fault Management, please refer to Intelligent Fault Management for T_{SOX} details.

5. TEMP

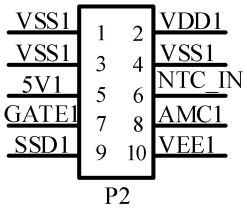
The pin which is used for the distributed NTC sampling, totally three different output choices: UART (all temperature from all modules), Frequency or Duty Cycle. Duty Cycle is the default setting for 2FHD0620.

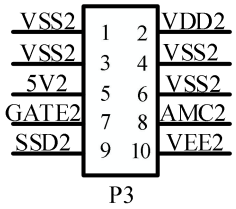
Temperature (℃)	Rntc (kΩ)	Duty cycle (%)
-40	99.092	6.0%
-35	75.144	8.0%
-30	57.533	10.0%
-25	44.448	12.0%
-20	34.610	14.0%
-15	27.156	16.0%
-10	21.483	18.0%
-5	17.120	20.0%
0	13.727	22.0%
5	11.082	24.0%
10	9.003	26.0%
15	7.359	28.0%
20	6.049	30.0%
25	5.000	32.0%
30	4.156	34.0%
35	3.472	36.0%
40	2.914	38.0%
45	2.458	40.0%
50	2.083	42.0%
55	1.773	44.0%
60	1.515	46.0%
65	1.300	48.0%
70	1.120	50.0%

75	0.968	52.0%
80	0.840	54.0%
85	0.732	56.0%
90	0.640	58.0%
95	0.561	60.0%
100	0.493	62.0%
105	0.435	64.0%
110	0.385	66.0%
115	0.342	68.0%
120	0.304	70.0%
125	0.271	72.0%
130	0.243	74.0%
135	0.217	76.0%
140	0.195	78.0%
145	0.176	80.0%
150	0.158	82.0%

Secondary Side Characteristics

1. Description of Secondary Side Interface





A 10-pin interface is equipped on both channels on the core board as P2 and P3. An extra pin in CH1 is used for the distributed NTC sampling.

CH1:

- 1x Secondary side ground V_{EE}
- 3x Secondary side negative voltage V_{SS}
- 1x Secondary side positive voltage V_{DD}
- 1x 5V supply
- 1x NTC sampling signal
- 1x Active Miller clamping signal AMC
- 1x Soft shut down signal SSD
- 1x Gate signal

CH2:

- 1x Secondary side ground V_{EE}
- 4x Secondary side negative voltage V_{SS}
- 1x Secondary side positive voltage V_{DD}
- 1x 5V supply
- 1x Active Miller clamping signal AMC
- 1x Soft shut down signal SSD
- 1x Gate signal

2. Secondary Side Ground V_{EE}

The V_{EE} terminal provides the reference ground for the secondary side.

3. Secondary Side Negative Voltage V_{SS}

The negative terminals Vss provide -9 to -0.5V voltage for the secondary side, which is related to the secondary side positive voltage V_{DD} and HW.

4. Secondary Side Positive Voltage V_{DD}

Positive voltage 15V-20V of secondary side, which is decided by the SW.

5. 5V Supply

5V power is used to power the logical circuit of adaptor board.

6. AMC, SSD, NTC_IN

Refer to Technical Principle.

Technical Principle

1. Power Supply and Electrical Isolation

The gate driver implements isolated power and signal. Power isolation is realized by the transformer, signal isolation is realized by capacitive coupling. The transformer complies with the safety isolation standard EN50178 and the primary and secondary sides fulfil protection class 2.

Please note that a stable supply voltage and current are required to power the driver.

2. Power Monitoring

The primary side of the driver, as well as the two secondary side power supplies, have local power detection circuits, as well as corresponding undervoltage protection.

When undervoltage occurs in the primary power supply, both channels are driven by the negative gate voltage to maintain the shutdown state (both channels are blocked), and both SO1 and SO2 feed back the fault status signal to the master computer.

When the positive or negative voltage on the secondary side is lower than the threshold voltage, the driver circuit will determine that an undervoltage fault has occurred, and the driver circuit will automatically block the MOSFET, and at the same time, the corresponding -SOx will feedback a fault signal to the master computer.

The SOx outputs are automatically reset after the primary and secondary undervoltage faults are removed.

Firstack recommends against operating either SiC in the bridge arm in an undervoltage state.

3. Intelligent Fault Management

The driver detects the operation status of the module in real time, and when the module fails, it uploads the fault status to the master computer through the SOx output, and the 2FHD0620 realizes the fault differentiation by the difference of the pull-down time of the SOx signal (the fault return time).

For more information, see the table below.

Fault Type	Short-circuit	Undervoltage(sec.)	Undervoltage(pri.)	Other Faults
Return time (Tsox)	10ms	20ms	40ms	80ms

4. SC Protection and Soft Shut Down TC/SSD

The 2FHD0620 is enable to detect the short-circuit during the operation of SiC module and start soft shut down to turn off the module safely. Currently the short-circuit protection detection is through the desaturation detection, of which there are two detection methods: resistance detection and diode detection, the 2FHD0620 adopts the latter.

The diode detection circuit can achieve high accuracy and fast reaction to protect the module during short circuit situation.

During the normal operation time the current will flow through the low impedance circuit consisting of diodes and resistors, which is used to limit the current. When the short-circuit occurs, the V_{ds} will increase due to the desaturation of the module, which will cause the reverse cut off of the diode, so that the current won't flow through the diode anymore and start charging the capacitor C1. After the charging time t_{RC} the voltage exceeds the threshold V_{ref}, the TC signal will be activated after a filter time t_{DS_FLT} and SSD signal will convert from low to high to start soft shut down function. In order to avoid the mis-trigger of SC protection during normal operation, a SCS filter time t_{BL} is specified by SW.

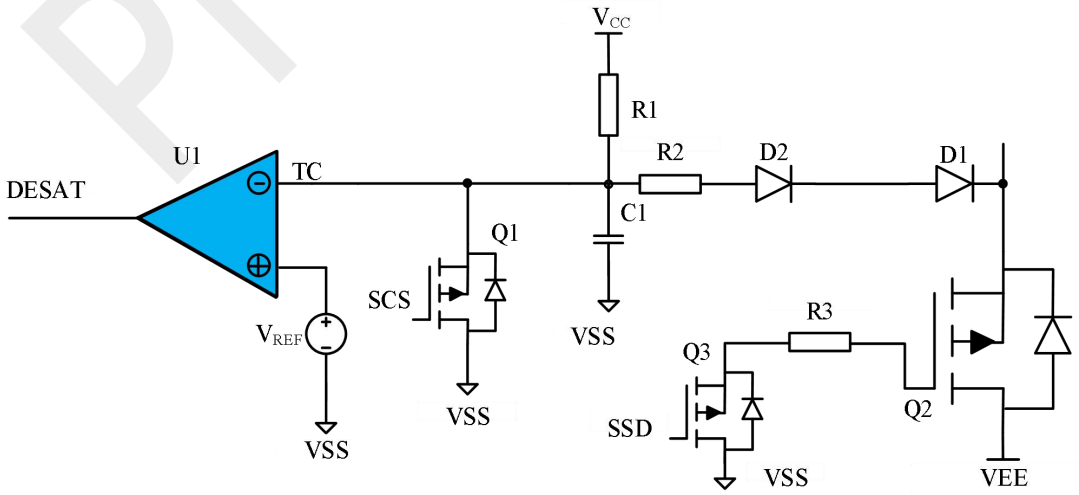


Fig.5 SC protection circuit

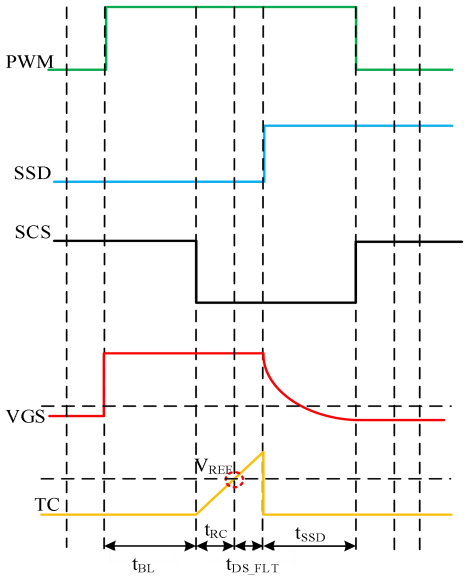


Fig.6 SC protection and SSD time sequence diagram

5. Active Miller Clamping (AMC)

The AMC is used to pull down the gate voltage to a certain negative voltage to suppress the over/undershoot caused by the high dv/dt of SiC MOSFET. Overshoot will lead to the short circuit and undershoot can damage the gate of module.

The AMC signal comes from the ASIC by Firstack. During the turn-on process the AMC signal will be low and after the filter time t_{AMC_ON} in the turn-off process the signal will convert to high to activate the miller clamping. The filter time t_{AMC_ON} can be modified by the SW. The default filter time of 2FHD0620 is 1.04μs, t_{AMC_OFF} is a stable 500ns.

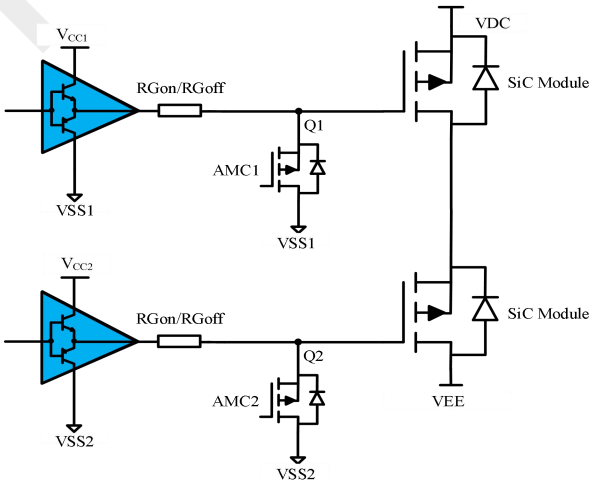


Fig.7 AMC circuit

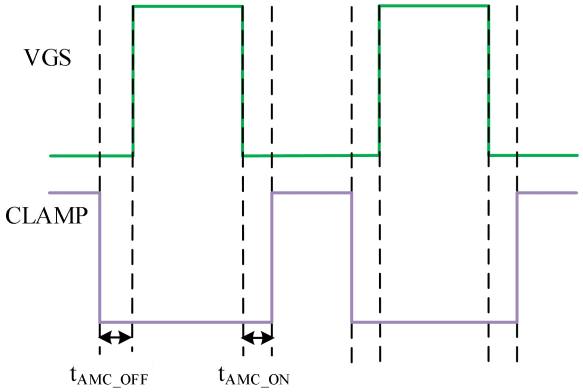


Fig.8 AMC time sequence diagram

6. Distributed NTC Sampling (NTC_IN)

The complete temperature information is important for customer to observe the operation status and optimize the architecture for heat dissipation. Therefore Firstack develops distributed NTC sampling circuit(DNTC). **Fig.9** introduces the basic topology. There are several advantages of this new design:

1. Temperature sampling from all modules
2. Communication between all GDUs based on the bus protocol
3. Highly robust and accurate temperature information
4. Uniform design for all kinds of modules

The distributed NTC will sample from the first adaptor board to the core board or the last adaptor board. During the transfer process, temperature information will be saved and transferred to the next microcontroller in sequence, and the last microcontroller will transfer all temperature or the highest temperature information depending on the software selection, and then output through the isolator.

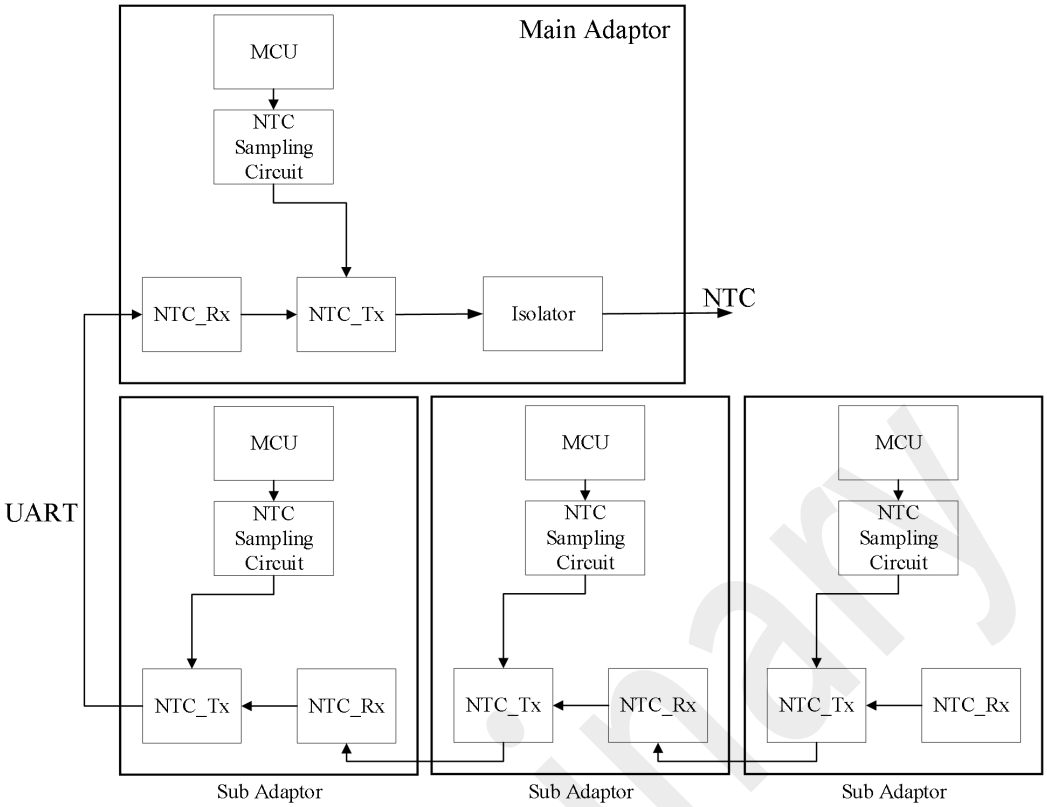


Fig.9 Distributed NTC sampling circuit topology

Technical Support

Firstack's professional team will provide you with business consultation, technical support, product selection, price, lead time and other related information, and guarantee to answer your questions within 48 hours.

Legal Disclaimer

This manual gives a detailed introduction about the product, but cannot promise to provide specific parameters. No warranty or guarantee, express or implied, is given herein as to the delivery, performance or applicability of the product.

Firstack reserves the right to modify technical data and product specifications at any time without prior notice. Firstack's general payment terms and conditions apply.

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