2FHC06M33XX

Application Manual

Gate driver core for SiC modules in parallel

The 2FHC06M33XX is a high-performance, dual-channel SiC gate driver core developed based on Firstack intelligent chip technology, supports SiC modules up to 3300V. The overall architecture consists of a MCC (main control core) and multiple MAB (module adaptor board) units, the MCC and MAB are connected by a set of cables, which can flexibly match 1~4 SiC modules.

The 2FHC06M33XX integrates driver protection, intelligent fault management, distributed NTC sampling and other functions, and is suitable for multi-parallel connection of packages such as Infineon XHP_2, Mitsubishi LV100, Hitachi Linpak and so on. The 2FHC06M33XX is mainly used in PV, wind, rail and other high reliability fields.

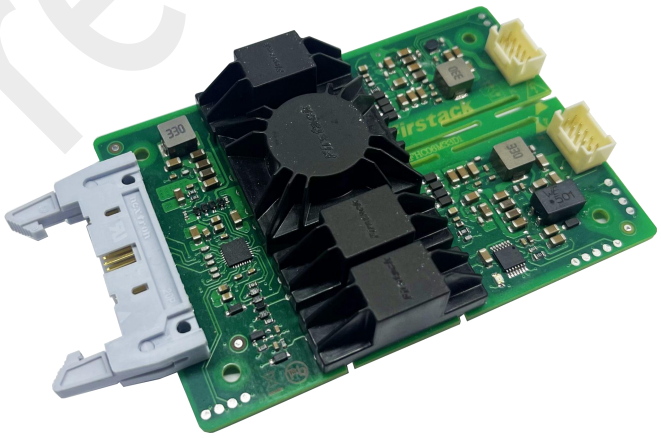
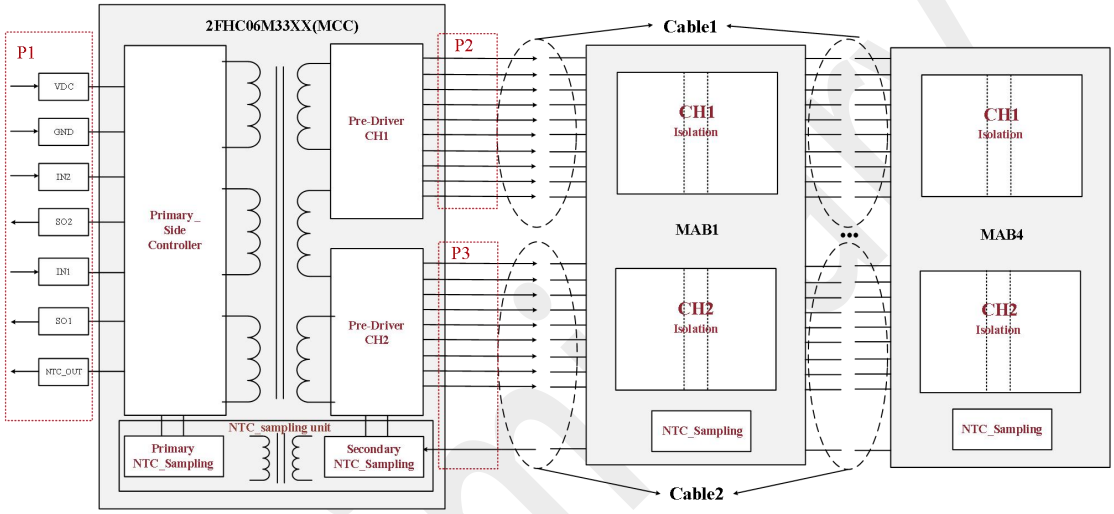


Fig.1 2FHC06M33XX

Contents

Abstract

The 2FHC06M33XX is a high performance, dual-channel gate driver developed by Firstack based on intelligent chip technology, and its overall architecture is shown in **Fig.2**. The 2FHC06M33XX needs to be used with module adaptor board (MAB), the MAB and the connecting cables are provided by Firstack. The gate driver can achieve up to four in parallel, and can be directly assembled without further development.



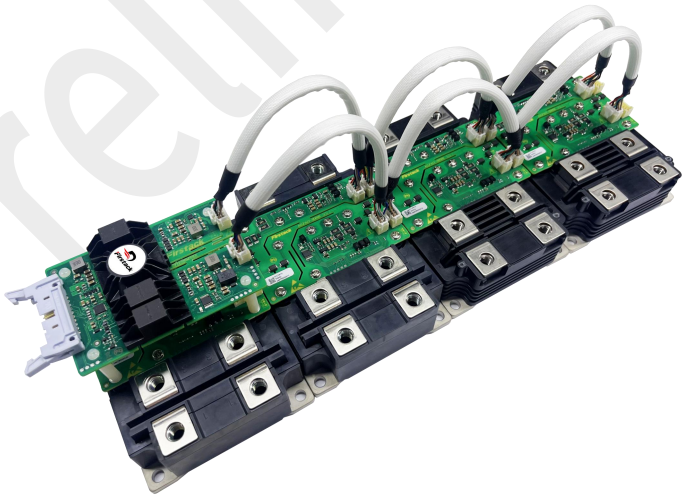


Fig.2 2FHC06M33XX architecture block diagram

Use Steps and Safety Notice

Simple use steps of the gate driver are as follows:

1. Choose suitable gate driver

When using the gate driver, pay attention to the model of the SiC module that the gate driver is adapted to. It is invalid for non-designated SiC modules. Improper use may cause the gate driver and the module failure.

2. Install the gate driver on the SiC module

Any treatment of SiC modules or gate drivers should follow the general specifications for the protection of electrostatic sensitive devices required by the international standard IEC 60747-1, Chapter IX or IEC 60340-5-2 (which means the workplace, tools, etc. must comply with these standards).

If these specifications are ignored, both the SiC module and the gate driver may be damaged.

3. Connect the gate driver to the control unit

Connect the gate driver connector to the control unit and input a suitable supply voltage to the gate driver.

4. Check the function of the gate driver

Check the gate voltage: for the turn-off state, the rated gate voltage is given in the corresponding data sheet. At this time moment the turn-on voltage will be different according to the modules. Please also check the input current of the gate driver with and without a control signal.

These tests should be performed before installation, because the gate terminal may not be accessible after installation.

5. Set up and test the power unit

Before starting the system, it is recommended to check each SiC module with a single pulse or double pulse test method. Firstack specially reminds: even under the worst conditions, it is

necessary to ensure that the SiC module does not exceed the operating range specified by SOA, because the operating condition of the SiC module strongly depends on the specific converter architecture.

Cable Description

With a set of cables 2FHC06M33XX is enable to be used for paralleling. There is prepared connectors for cables on the core board. Customer only needs to choose the suitable length of cable by actual application.

Note: The cable is special designed for corresponded product, if customer uses their own cables, Firstack can not promise the performance.

Part Number	Cable Length (mm)	Pin Definition
JWDET-00618	200	3rd pin as ground
JWDET-00810	100	

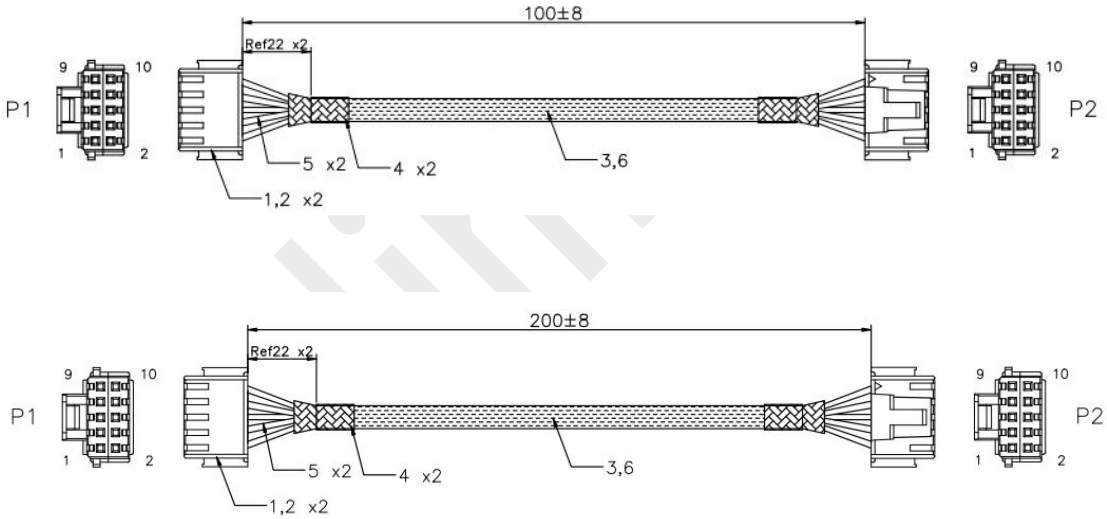
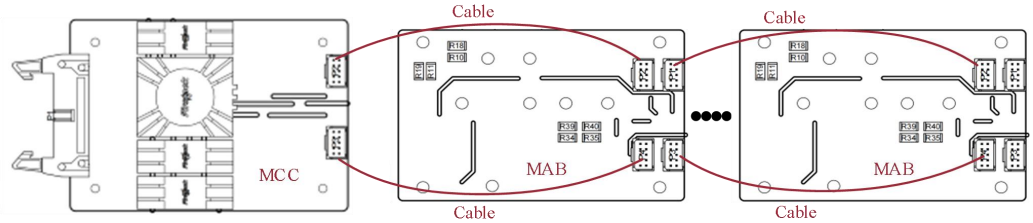


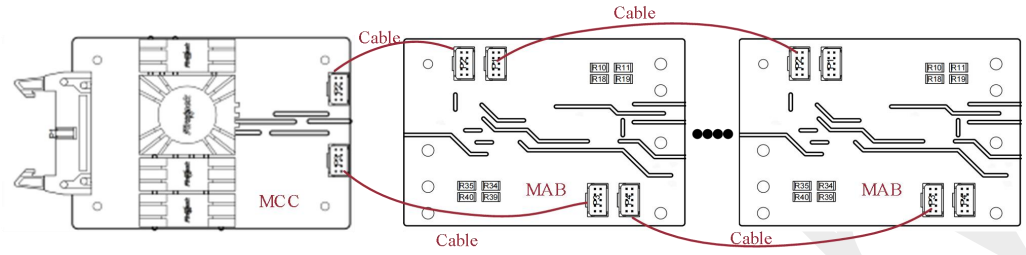
Fig.3 3D diagram of cables

Assemble/Disassemble Description

The MAB are mounted on the module by M3 screws, MCC is placed in the corresponding position according to the design structure, which meets the insulation requirements, MCC and MAB need to be connected in strict accordance with the following diagram.



2FHC06M33XX+A1LPA1V-S0002 parallel connection diagram



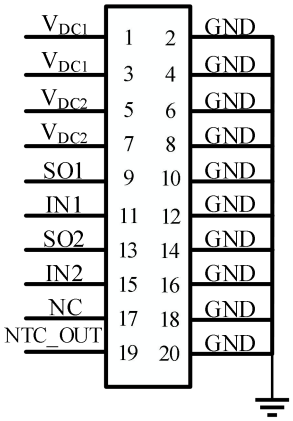
2FHC06M33XX+A1XHPA1V-S0001 parallel connection diagram

Fig.4 Parallel connection diagram

Primary Side Characteristics

1. Description of Primary Side Interface

The primary side interface of 2FHC06M33XX is a 20-pin ejector header on the adaptor board:



P1

- 4x power supply terminals V_{DC} (pin1 and 3 are 24V power supply pins, pin5 and 7 are 15V power supply pins, only one power supply method can be selected)
- 2x drive signal input INx
- 2x fault signal output SOx
- 10x GND (ground)
- 1x NTC_OUT
- 1x NC (free)

2. V_{DC}

The 2FHC06M33XX is configured with 2 kinds of V_{DC} power supply terminals for supplying power to the primary side circuit and the isolated DC/DC converter to provide positive and negative voltages to the secondary side. (pin1 and 3 are 24V power supply pins, and pin5 and 7 are 15V power supply pins, only one power supply method can be selected) The maximum supply current required by the 15V supply main control board is 120mA.

3. INx

The signal input pin of the gate driver, supports 3.3-15V logic level, the default setting is 15V

output. The function of INx is related to the driving mode, which is selected by software(SW), and cannot be adjusted by hardware(HW).

Direct Mode:

IN1 and IN2 are independent signals. CH1 and CH2 can be turned on simultaneously.

Half-bridge topology: To avoid CH1 and CH2 both in high voltage level, which causes the short-circuit, the dead time must be enough set by control circuit.

Half-bridge Mode:

IN1 is the input terminal of drive signal (PWM), IN2 is the enable terminal (EN);

IN2 is low level, two outputs are blocked, all output signals are low level.

IN2 is high level, two outputs are enabled, output signals are changed follow the changing of IN1.

When IN2 is high level, IN1 converts from high to low level, the gate signal of CH2 is blocked immediately and turns on after dead time T_d.

Attention: The default mode of 2FHC06M33XX is direct mode. By using half-bridge mode the dead time T_d can be adjusted by SW, inaccessible by external sources. After a dead time during the process of IN2 from low to high, the output can follow the changing of IN1.

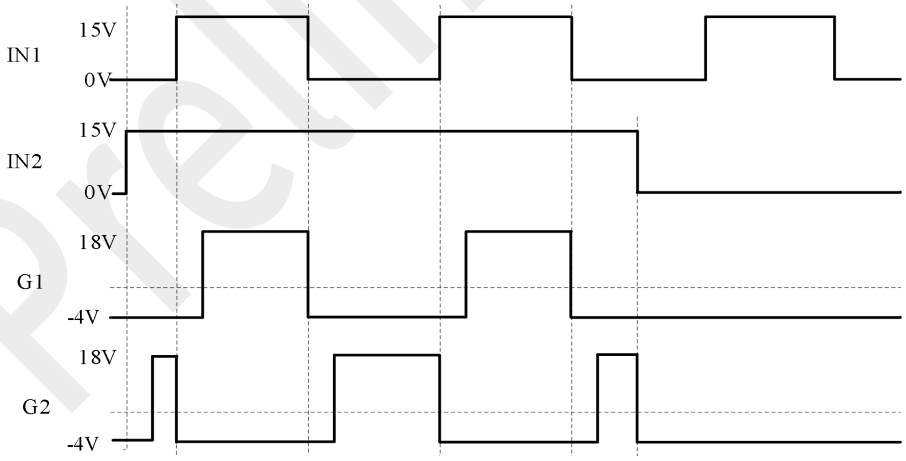


Fig.5 Logic diagram of half-bridge mode

4. SO1, SO2 Status Output

The SOx is the transistor drain with a 4.7K pull-up resistor and defaults to a separate fault signal in order to pinpoint the problem. They can also be connected together to provide common fault

signal.

When channel “x” detects fault, SOx will be low (connected to GND).

SOx Output Logic

When an undervoltage occurs in primary side, the gate will be negatively turned off directly and keep blocking for a blocking time, at the same time both SOx goes to high after report 40ms low level fault.

If the undervoltage disappears before above process, SOx will keep high. If the undervoltage still occurs, the fault will be pulled down again until the fault disappears, then return to high after a blocking time (80ms).

Primary side blocking signal: after the primary side undervoltage fault disappears and another 80ms, the blocking is over, primary side will process the INx signal normally.

When an undervoltage occurs in secondary side of the gate driver, the gate performs soft shut down first and keeps blocking signal, the corresponding SOx signal reports 20ms low level fault and after that returns to high level 100ms.

If the undervoltage disappears before the above process, SOx keep high; if the fault still occurs, the signal will be pulled down again until the fault disappears, then after another 80ms the SOx signal returns to high level.

Primary side blocking signal: after the secondary side undervoltage fault disappears, then after 80ms the blocking is over, primary side will process the INx signal normally.

When a short-circuit fault occurs on the secondary side of the gate driver, the gate first performs the soft shut down, then puts in a negative voltage to keep the shutdown state and maintains blocking signal, the corresponding SOx signal reports the fault, and then automatically restores the high level after pulling it down for 10ms.

The 2FHC06M33XX is equipped with Intelligent Fault Management, please refer to Intelligent Fault Management for T_{SOX} details.

5. TEMP

The pin which is used for the distributed NTC sampling, totally three different output choices:

UART (all temperature from all modules), Frequency or Duty Cycle. Duty Cycle is the default setting, which output the highest channel temperature. Its NTC resistance versus duty cycle is shown in Table 1.

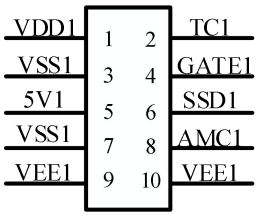
Temperature(℃)	Rntc(kΩ)	Duty Cycle (%)
-40	99.092	6.0%
-35	75.144	8.0%
-30	57.533	10.0%
-25	44.448	12.0%
-20	34.610	14.0%
-15	27.156	16.0%
-10	21.483	18.0%
-5	17.120	20.0%
0	13.727	22.0%
5	11.082	24.0%
10	9.003	26.0%
15	7.359	28.0%
20	6.049	30.0%
25	5.000	32.0%
30	4.156	34.0%
35	3.472	36.0%
40	2.914	38.0%
45	2.458	40.0%
50	2.083	42.0%
55	1.773	44.0%

60	1.515	46.0%
65	1.300	48.0%
70	1.120	50.0%
75	0.968	52.0%
80	0.840	54.0%
85	0.732	56.0%
90	0.640	58.0%
95	0.561	60.0%
100	0.493	62.0%
105	0.435	64.0%
110	0.385	66.0%
115	0.342	68.0%
120	0.304	70.0%
125	0.271	72.0%
130	0.243	74.0%
135	0.217	76.0%
140	0.195	78.0%
145	0.176	80.0%
150	0.158	82.0%

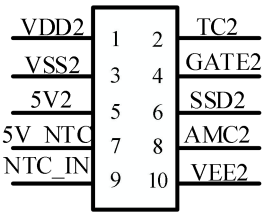
Table 1 NTC resistance and duty cycle

Secondary Side Characteristics

1. Description of Secondary Side Interface



P2



P3

The secondary side of the gate driver has 2 channels CH1 and CH2, each with a 10-pin interface terminal P2, P3. An extra pin in CH2 is used for the distributed NTC sampling.

CH1:

- 2x Secondary side ground V_{EE}
- 2x Secondary side negative voltage V_{SS}
- 1x Secondary side positive voltage V_{DD}
- 1x 5V supply
- 1x TC signal
- 1x Active Miller clamping signal (AMC)
- 1x Soft shut down signal (SSD)
- 1x Gate signal

CH2:

- 1x Secondary side ground V_{EE}
- 1x Secondary side negative voltage V_{SS}
- 1x Secondary side positive voltage V_{DD}
- 1x 5V supply
- 1x NTC supply
- 1x TC signal
- 1x Active Miller clamping signal (AMC)
- 1x Soft shut down signal (SSD)
- 1x Gate signal

- 1x NTC sampling input signal

2. Secondary Side Ground V_{EE}

The V_{EE} provides the reference ground for the secondary side.

3. Secondary Side Negative Voltage V_{SS}

The Vss provides -9 ~ -0.5V negative voltage for the secondary side, which can be set with reference potential V_{EE}.

4. Secondary Side Positive Voltage V_{DD}

The V_{DD} provides 15~20V for the secondary side, which can be set with reference potential V_{EE}.

5. 5V Supply

Provide 5V to the module adaptor board logic circuits with reference potential V_{SS}.

6. 5V_NTC

Provide 5V to the NTC sampling circuit with reference potential V_{EE}.

7. TC, AMC, SSD, NTC_IN

Refer to the Technical Principle.

Technical Principle

1. Power Supply and Electrical Isolation

The gate driver implements isolated power and signal. Power isolation is realized by the transformer, signal isolation is realized by capacitive coupling. The transformer complies with the safety isolation standard EN50178 and the primary and secondary sides fulfil protection class 2.

Please note that a stable supply voltage and current are required to power the driver.

2. Power Monitoring

The primary side of the gate driver, as well as the two secondary side power supplies, have local power detection circuits and corresponding undervoltage protection.

When the undervoltage occurs in the primary side power supply, both SiC are driven by the negative gate voltage to maintain the turn-off state (both channels are blocked), and both SO1 and SO2 feed back the fault status signal to the master computer.

When the positive or negative voltage on the secondary side is lower than the threshold voltage, the drive circuit will determine that an undervoltage fault has occurred, and will automatically block the SiC, at the same time, the corresponding SOx will feedback a fault signal to the master computer.

The SOx will automatically reset after the primary and secondary side undervoltage disappear.

Firstack recommends any SiC in the bridge arm should not operate in an undervoltage state.

3. Intelligent Fault Management

The gate driver detects the operation status of the module in real time. When the module fails, it uploads the fault status to the master computer through the SOx, and the 2FHC06M33XX realizes the fault differentiation by the difference of the pull-down time (fault return time) of the SOx.

For more information, see the table below.

Fault Type	Short-circuit	Undervoltage(sec.)	Undervoltage(pri.)	Other Faults
Return time (Tsox)	10ms	20ms	40ms	80ms

4. SC Protection and Soft Shut Down(TC, SSD)

The 2FHC06M33XX is enable to detect the short-circuit during the operation of SiC module and start soft shut down to turn off the module safely. Currently the short-circuit protection detection is through the desaturation detection, of which there are two detection methods: resistance detection and diode detection, the 2FHC06M33XX adopts the latter.

The diode detection circuit enables high accuracy and fast response to protect the module in case of short-circuit.

During the normal operation the current will flow through the low impedance circuit consisting of diodes and resistors, which is used to limit the current. When the short-circuit occurs, the V_{ds} will increase due to the desaturation of the module, which will cause the reverse cut off of the diode, so that the current won't flow through the diode anymore and start charging the capacitor C1. After the charging time t_{RC}, the voltage exceeds the threshold V_{ref}. The TC signal will be activated after a filtering time t_{DS_FLT} and the DESAT signal will convert from low to high to start soft shut down. In order to prevent the short-circuit protection function from being triggered by mistake when DS falls at the turn-on moment, a certain SCS time t_{BL} needs to be set.

When a short-circuit is detected, the gate signal will be in a high impedance state, the SSD signal will be set high, and Q3 will be turned on, so that the current will flow through the SSD resistor R3 to realize soft shut down, thus effectively suppressing the turn-off peaks brought about by high di/dt.

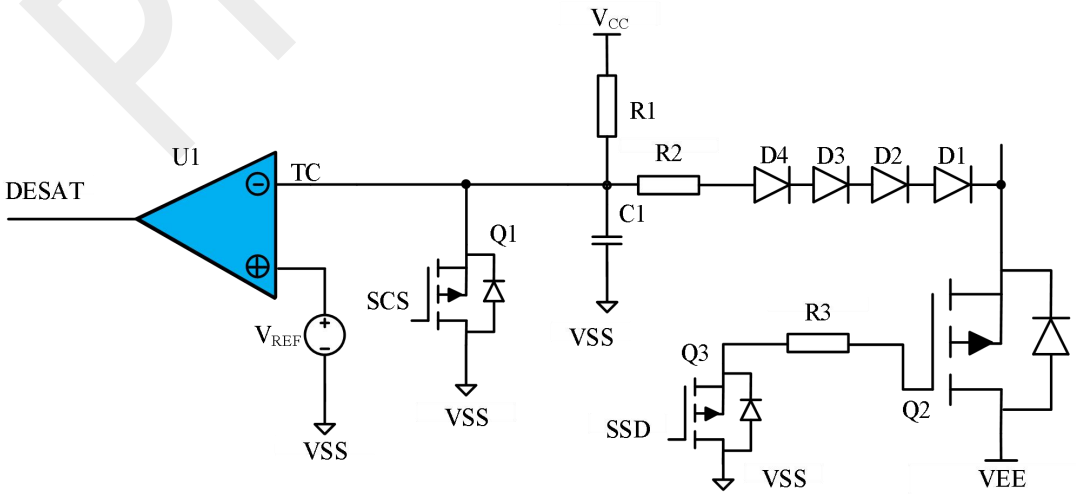


Fig.6 Short-circuit protection detection circuit

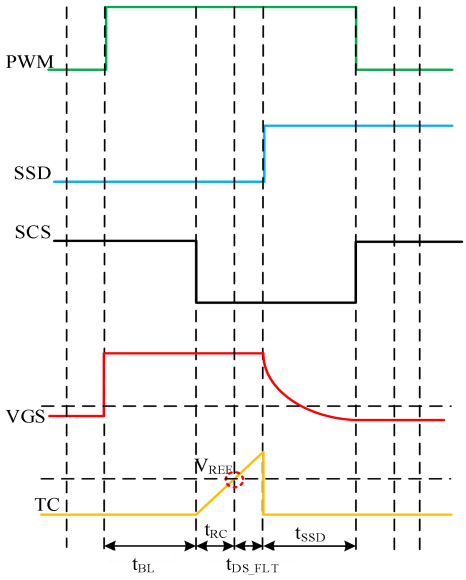


Fig.7 SC protection and SSD time sequence diagram

5. Active Miller Clamping (AMC)

The AMC will pull down the gate voltage to a certain negative voltage to suppress the half-bridge crosstalk caused by the high dv/dt of SiC. Overshoot will lead to the short-circuit and undershoot can damage the gate.

The AMC signal comes from the ASIC of Firstack. During the turn-on process the AMC signal is low; during the turn-off process, after the filtering time t_{AMC_ON} the signal will turn to high to activate the Miller clamping. The filtering time t_{AMC_ON} can be set by the SW. The default filtering time of 2FHC06M33XX is 1.56μs, t_{AMC_OFF} is a stable 500ns.

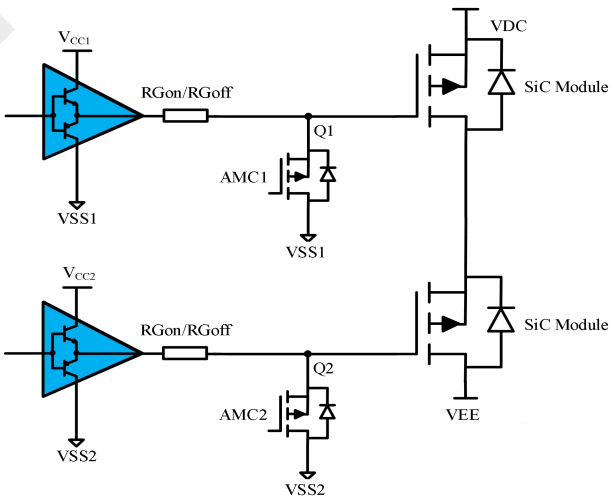


Fig.8 AMC circuit

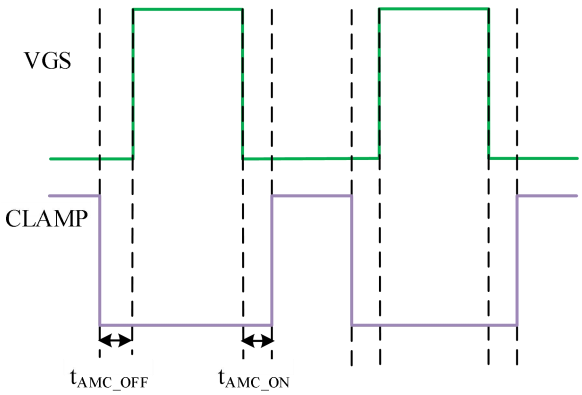


Fig.9 AMC time sequence diagram

6. Distributed NTC Sampling (NTC_IN)

For packaged modules such as Infineon XHP_2, Mitsubishi LV100, Hitachi Linpak, etc., negative temperature coefficient resistors (NTC) are integrated internally, one end of which is connected to the source (S) of the bottom bridge arm of the module, the isolation sampling is required. Firstack has developed a distributed NTC (DNTC) sampling circuit for this purpose, which samples from the first MAB to the MCC or the last MAB. During the transmission process, the temperature information will be saved and sequentially transmitted to the next microcontroller, and the last microcontroller will transmit all the temperature or the highest temperature information according to the SW and report it to the master computer, which is convenient for the user to check the operation status and optimize the architecture for heat dissipation. **Fig.10** describes the basic topology of the circuit, and this new design has several advantages:

1. Temperature sampling from all modules
2. Communication between all GDUs based on the bus protocol
3. Highly robust and accurate temperature information
4. Uniform design for all kinds of modules

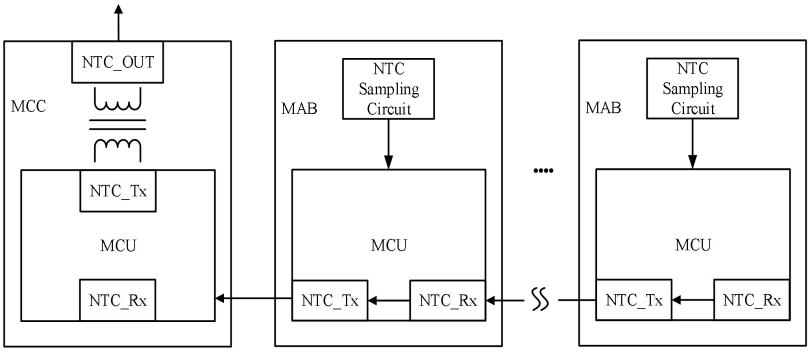


Fig.10 Distributed NTC sampling circuit topology

Technical Support

Firstack's professional team will provide you with business consultation, technical support, product selection, price, lead time and other related information, and guarantee to answer your questions within 48 hours.

Legal Disclaimer

This manual gives a detailed introduction about the product, but cannot promise to provide specific parameters. No warranty or guarantee, express or implied, is given herein as to the delivery, performance or applicability of the product.

Firstack reserves the right to modify technical data and product specifications at any time without prior notice. Firstack's general payment terms and conditions apply.

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