2FHC0215xV

Application Manual

Compact gate driver core, supports multi-level

The 2FHC0215xV is a dual-channel gate driver with electrical interface. It is also with ASIC digital control for safe and reliable driving of IGBT. The gate driver is suitable for all common IGBT up to 900A/1700V and supports multi-level topology.

The 2FHC0215 is a vertical plug-in driver core with dimensions of 71mm*35mm and a maximum height of 16mm.

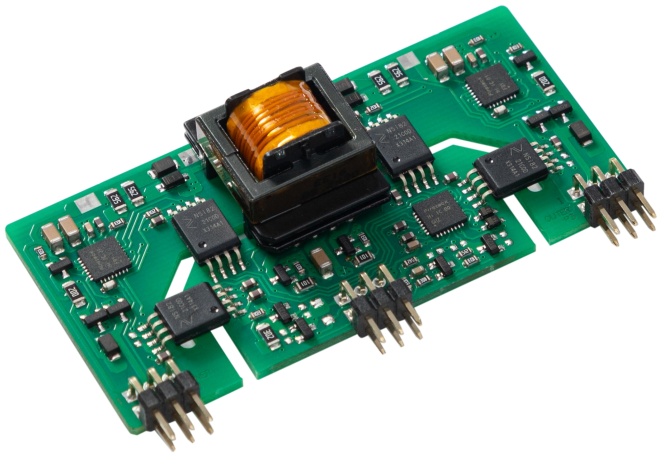


Fig.1 2FHC0215xV

Contents

Driver Overview

The 2FHC0215xV is a compact gate driver core developed by Firstack based on digital control, the target market is the low to medium power, dual-channel IGBT applications such as general purpose inverters, UPS, power quality, and so on.

The 2FHC0215xV contains a complete dual-channel IGBT driver core with isolated DC/DC converter, short-circuit protection and supply voltage monitoring with SSD.

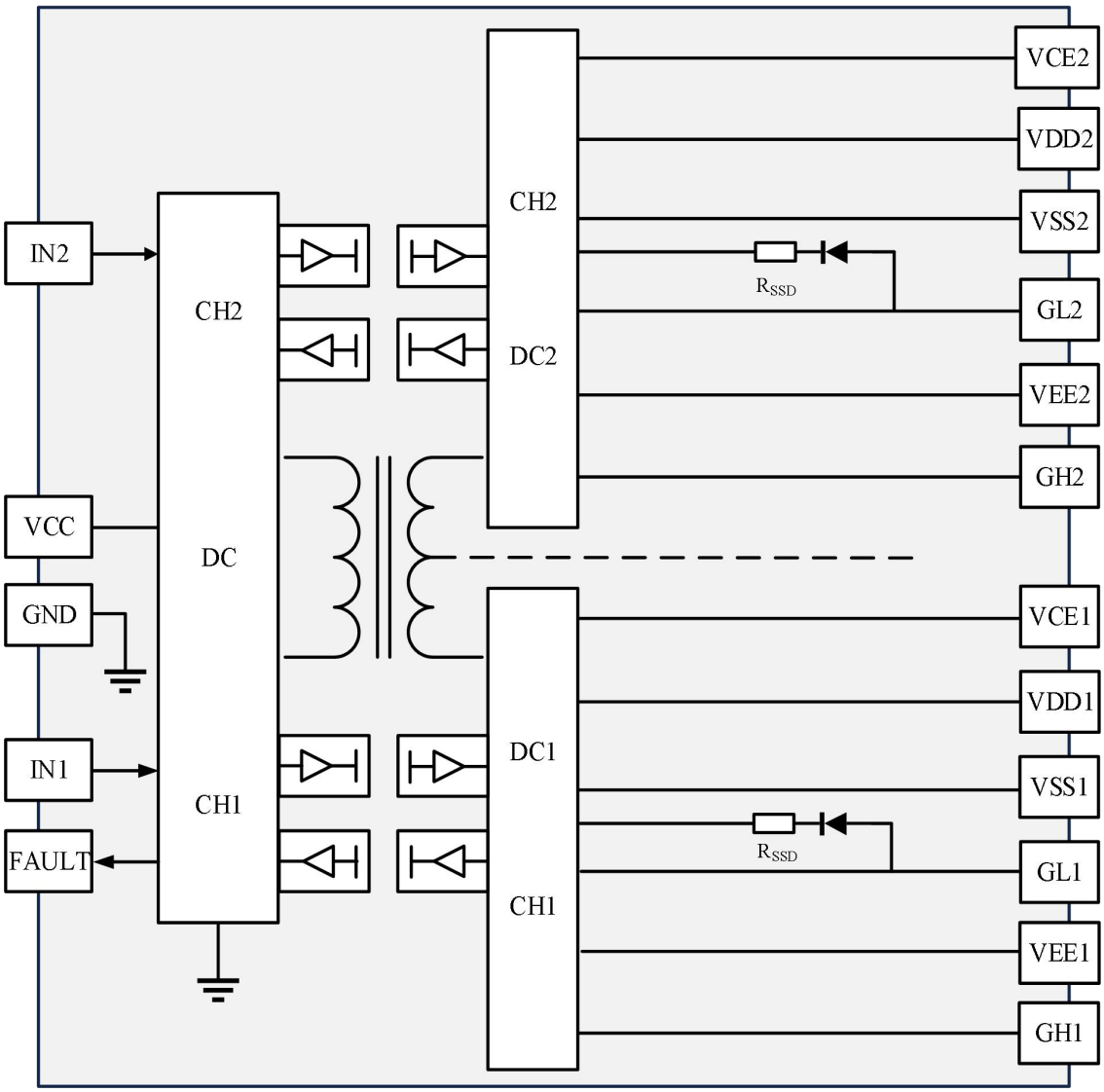


Fig.2 2FHC0215xV block diagram

Pin Designation

Pin	Definition	Function
Primary Side-P2		
1	FAULT	Fault output channel, normal high-impedance, 0V on fault
2	IN1	Signal input, channel 1
3	NC	Free
4	IN2	Signal input, channel 2
5	GND	Ground
6	VCC	Supply voltage, 15V supply for primary side
Secondary Side-P1		
1	VDD2	Positive supply channel 2
2	VSS2	Negative supply channel 2
3	GL2	Gate low channel 2; pulls gate low through tum-off resistor
4	VCE2	V_{CE} sense channel 2
5	GH2	Gate high channel 2; pulls gate high through tum-on resistor
6	VEE2	Emitter (reference ground) channel 2
Secondary Side-P3		
1	VDD1	Positive supply channel 1
2	VSS1	Negative supply channel 1
3	GL1	Gate low channel 1; pulls gate low through tum-off resistor
4	VCE1	V_{CE} sense channel 1
5	GH1	Gate high channel 1; pulls gate high through tum-on resistor
6	VEE1	Emitter (reference ground) channel 1

Description of Primary Side Interface

Recommended Interface Circuitry for the Primary Side Connector

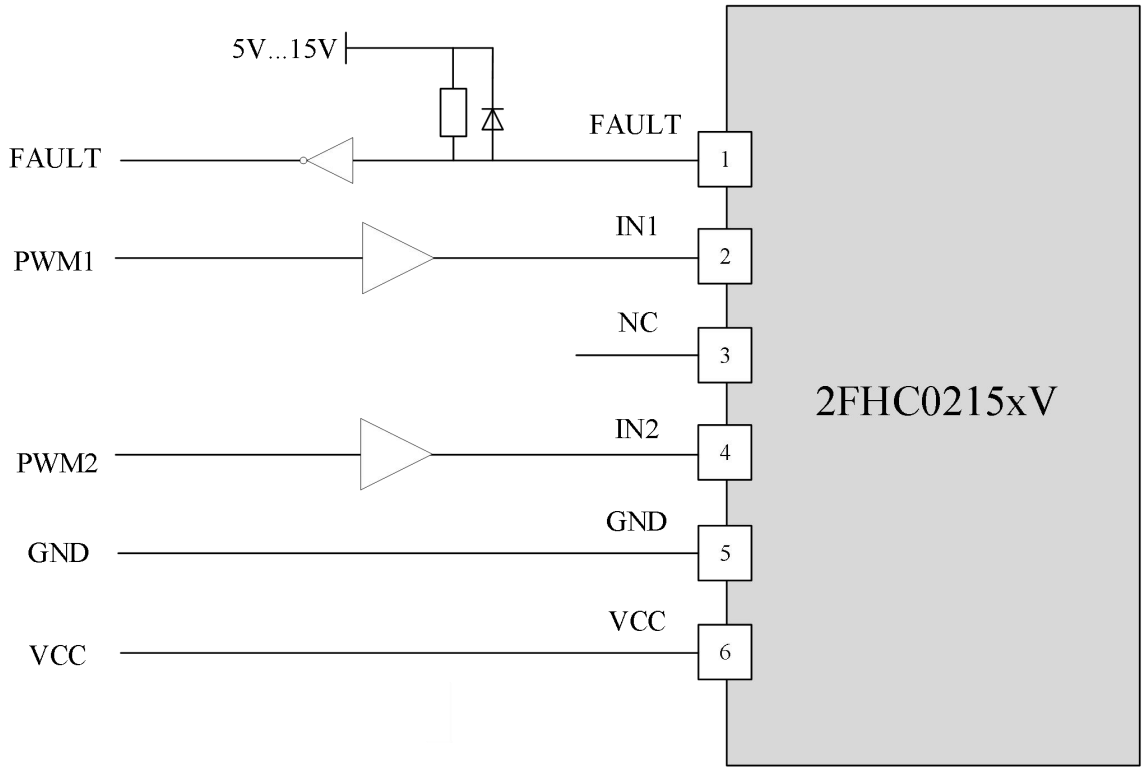


Fig.3 Recommended user interface of 2FHC0215xV (primary side)

Description of Primary Side Interface

The primary side interface of the 2FHC0215xV is quite simple and easy to use.

Primary side is equipped with a 6-pin interface connector with the following terminals:

- 1x power supply
- 2x driving signal inputs
- 1x fault status output
- 1x GND (ground)
- 1x NC (free)

V_{CC}

The 2FHC0215xV is equipped with a VCC terminal to supply power to both primary side circuit and isolated DC/DC converter and provide positive and negative voltage to the secondary side. The maximum current of the gate driver is 450mA.

INx

The signal input pin of the gate driver, supports 5-15V logic level, the resistance matching is important during design process.

IN1 and IN2 are independent. CH1 and CH2 can be turned on at the same time.

FAULT Status Output

The output FAULT is in the form of an open-drain transistor with only one terminal providing the common fault signal.

The value of the current flowing through the FAULT during the fault condition must not exceed the 10mA specified in the data sheet.

When there is no fault detected, the output is high resistance, the pull-up resistor is required to install in main control board. The recommended range of pull-up voltage is 5-15V, resistor value: 5V---3.3k~4.7k, 15V---10k~15k.

Output Logic - Primary Side Fault

In the event of an undervoltage fault on the primary side of the gate driver, the gate is shut down directly at negative voltage.

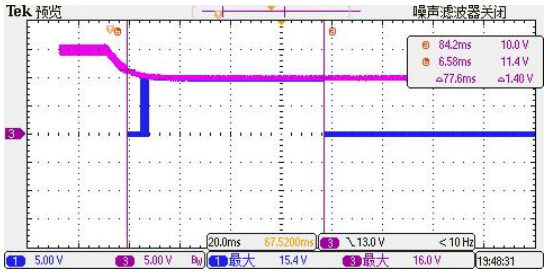


Fig.4 Fault occurrence logic

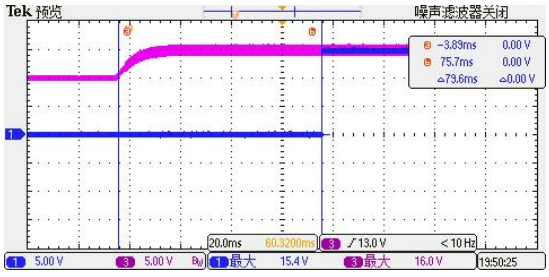


Fig.5 Fault disappearance logic

The time of primary side undervoltage fault can be divided into three periods: 1. fault occurs, 2. fault persists, 3. fault disappears.

1. Fault occurs: FAULT pin is pulled to low level for 5ms, then the output fault coding time lasts for 3ms, and the high level is restored for 72ms; as **Fig.4**

2. Fault persists: if the primary side undervoltage fault persists, the FAULT is always low; as **Fig. 4**

3. Fault disappears: when the primary side undervoltage disappears, after another 80ms, the FAULT signal is restored to high level; as **Fig.5**

Primary side blocking signal: when the primary side undervoltage fault disappears, after another 80ms, the blocking ends and the primary side processes INx signal normally.

Output Logic - Secondary Side Fault

When an undervoltage fault occurs on the secondary side of the gate driver, the gate first performs soft shut down, and then puts in a negative voltage for a certain period of time before keeping 0V turn-off and maintaining the blocking signal. After the disappearance of the undervoltage fault on the secondary side, and another blocking time (80ms), the blocking ends, and the primary side processes the INx signal normally.

Since the communication forms a fault code, a fault code transfer is present in the FAULT output.

When the ASIC chip detects a fault, it will first pull down for 5ms, and then followed by the output of 3ms fault code, a total of 8ms fault output, the 5ms + 3ms fault output signal is called a "fault signal" for the convenience of description.

The actual decoding only needs to detect the low level for 5ms, 3ms fault code is only used for internal communication of the gate driver, which has no impact on the actual application, and can be ignored without processing.

Secondary Side Undervoltage fault:

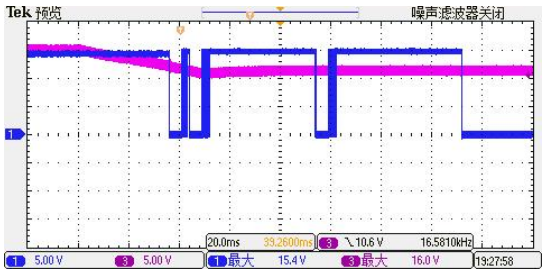


Fig.6 Fault occurs

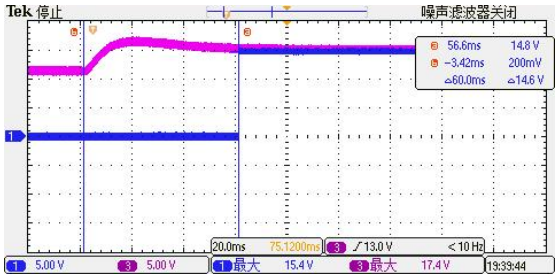


Fig.7 Fault disappears

1. Undervoltage occurs: FAULT pin outputs 2 "fault signal", then goes high level for 44ms; outputs the "fault signal" once more and sets high for 52ms; as **Fig.6**

2. Fault persists: if the secondary side undervoltage fault persists, the FAULT is always low; as **Fig.6**

3. Fault disappears: when the secondary side undervoltage disappears, keep low for up to 60ms, and then restore the high level; as **Fig.7**

Short-circuit fault:

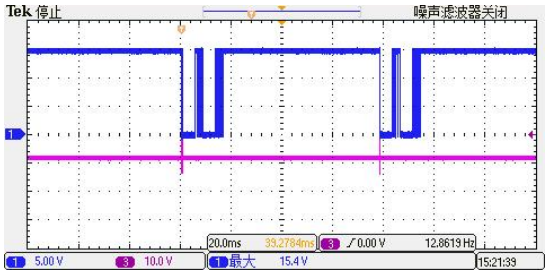


Fig.8 Short-circuit occurs

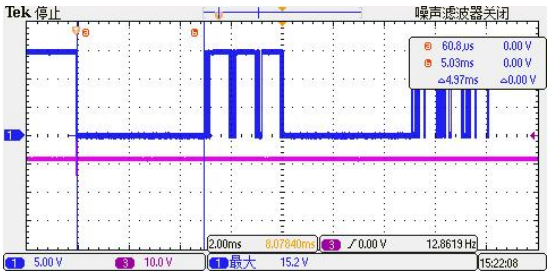


Fig.9 Fault signal

A short-circuit occurs in any channel: FAULT outputs the "fault signal" twice, then the fault is always high, as **Fig.8**.

The details of the fault signal are shown in **Fig.9**.

Description of Secondary Side Interface

Recommended Interface Circuitry for the Secondary Side Connector

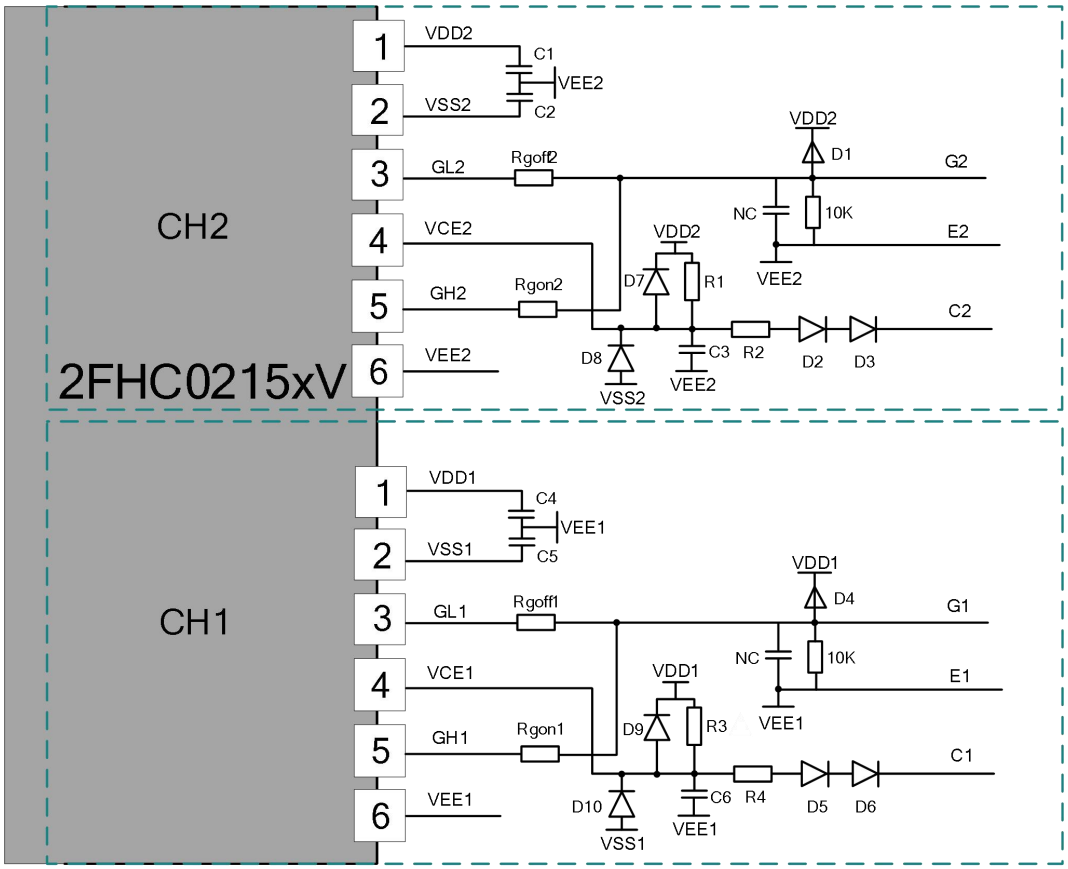


Fig.10 Recommended user interface of 2FHC0215xV (secondary side)

Description of Secondary Side Interface

Secondary side is equipped two channels CH1 and CH2 with a 6-pin interface connector with the following terminals respectively:

- 1 x positive power supply VDDx
- 1 x negative power supply VSSx
- 1 x emitter VEEx
- 1 x collector sense VCEx
- 1 x gate turn-on GHx
- 1 x gate turn-off GLx

Positive & Negative Power Supply (VDDx & VSSx) and Emitter Terminal VEEx

The gate driver is designed for extensibility, leading out the positive power supply VDDx, negative power supply VSSx, and emitter terminal VEEx.

For IGBTs with a gate charge of 3uC or less, the secondary side can be driven without additional support capacitor. For IGBTs with gate charge exceeding 3uC, the external support capacitor needs to be increased by 3uF for every 1uC increase, placed between VDDx-VEEx and VEEx-VSSx. These two support capacitors must be placed as close as possible to the gate driver terminals to reduce the loop inductance. It is recommended to use ceramic capacitors with a withstand voltage of 25V or more, and the same capacitance value is recommended.

The emitter terminal must be connected to the auxiliary emitter of the IGBT according to the circuit of **Fig.10**.

Collector Sense Terminal (VCEx)

The 2FHC0215xV collector potential sense supports diode sense and needs to be connected to the collector of the IGBT in accordance with the corresponding recommended circuit to detect a short-circuit in the IGBT.

When the IGBT is turned off, GHx is turned off and GLx is turned on, and the gate voltage is the VSSx potential. The chip internally sets the VCEx pin to the VSSx potential, and at this time, the capacitor Cax is discharged to the negative supply voltage, and this capacitor has a voltage of about -8V with respect to VEEx.

During the turn-on process and conduction state of the IGBT, GHx is turned on and GLx is turned off, the gate voltage is +15V, which charges the capacitor Cax through Rax, and the voltage of Cax increases. When the collector voltage of the IGBT decreases to a certain potential, the voltage of Cax is clamped by the high voltage diode D1x.

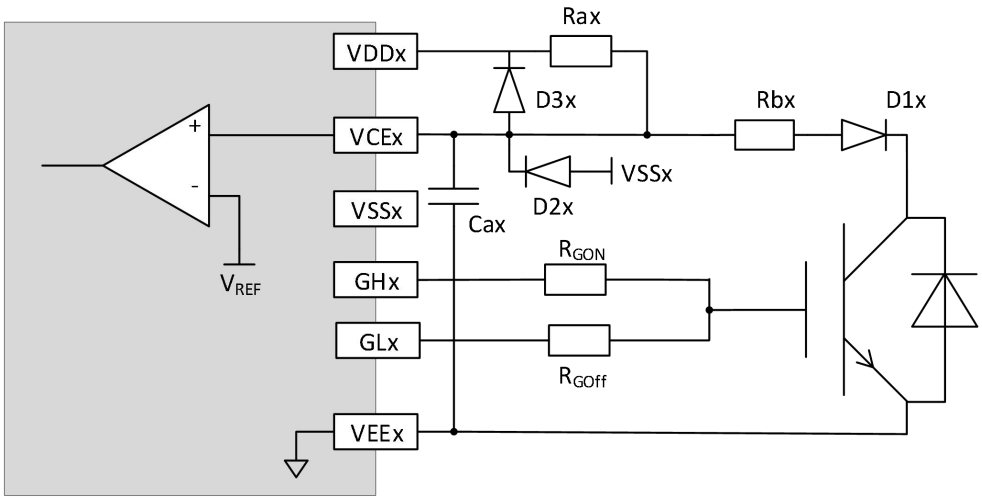


Fig.11 Diode sense reference circuit

The default VREF value for the 2FHC0215xV is 10V.

Recommended circuit component parameters are listed below:

D1x: 2 US1M, used for 1200V IGBT

2~3 US1M, used for 1700V IGBT

D2x, D3x: fast recovery diodes, e.g. BAS316, require low leakage current and cannot use Schottky

Rax: 5KΩ, two or more 1206 resistors of equal power in parallel are recommended

Rbx: 100Ω~330Ω

Cax: 0-10pF

Cax needs to consider the suppression diode D2x and the parasitic capacitance of the PCB.

Description: adjusting Cax can adjust the response time of the short-circuit protection.

Cax ↑ ⟶ TSC ↑

Recommended parameters: Cax=10pF, Rax=5kΩ

T_{SC_CH1}=6.7us T_{SC_CH2}=8.5μs

Shield V_{CE} Sense

The gate driver design using the diode detection circuit, if the gate driver is given a turn-on signal without the module connected, the gate driver will report a short-circuit fault, at this time, the function of shielding V_{CE} sense can be achieved by shorting Cx and Ex (refer to **Fig.10** for the

recommended circuit on the secondary side)

Gate Drive Terminal (GHx & GLx)

The gate driver connects a resistor to the gate of the IGBT through the gate drive terminal. The GHx and GLx pins control the turn-on and turn-off of the IGBT respectively, and the turn-on and turn-off resistors can be set separately as required. Please refer to **Fig.10** for design.

It is recommended to connect a 10k to 22k resistor between Gx and VEx. This resistor can provide a low impedance loop between the IGBT gate and emitter in case of the gate driver power down, and avoid floating voltage which causes IGBT false turn-on.

Under IGBT short-circuit conditions, the too high V_{GE} will result in excessive short-circuit current, a normal diode (D1/D4) needs to be connected between the gate and V_{DD} to clamp, and do not use a Schottky diode, please refer to **Fig.10** for the circuit.

Please note that in half-bridge circuits, it is recommended not to generate waveforms for switching action of the IGBTs with a low supply voltage to the gate driver, otherwise a too high change rate of VCE may lead to partial conduction of the IGBTs.

Technical Principle

Power Supply and Electrical Isolation

This gate driver implements isolated power and signal. Power isolation is realized by the transformer, signal isolation is realized by capacitive coupling. The transformer complies with the safety isolation standard EN50178 and the primary and secondary sides fulfil protection class 2.

Please note that a stable supply voltage and current are required to the gate driver.

Power-Supply Monitoring

The primary side of the gate driver, as well as the two secondary side power supplies, have local power sense circuits and corresponding undervoltage protection.

When an undervoltage occurs at the power supply of the primary side, both IGBTs are driven by the negative gate voltage to maintain the turn-off state (both channels are blocked), and FAULT feeds back the fault status signal to the master computer.

When the positive or negative voltage of the secondary side is lower than the threshold voltage, the drive circuit will determine that an undervoltage has occurred, and automatically block the IGBT. At the same time, FAULT will feedback a fault signal to the master computer.

The SOx outputs will automatically reset after the primary and secondary side undervoltage disappears.

Firstack recommends that any IGBT in the bridge arm should not operate in an undervoltage state.

Due to the presence of C_{CG}, when one IGBT in the bridge arm turns on, the high dv/dt from it can be coupled to the other IGBT through the C_{CG}, resulting in partial conduction of the other IGBT.

Soft Shut Down (SSD)

The full range of 2FHC0215xV gate drivers feature SSD function.

When the IGBT desaturation occurs, VCE reaches the bus voltage. At the same time, the IC will reach 4 times of the rated current or even more and the di/dt at the turn-off time will form a very high voltage peak on the parasitic inductance, which will easily damage the IGBT.

When the IGBT desaturation is triggered, the digital core will detect and trigger soft shut down to turn off the IGBT. Within 10us, the IGBT is gradually turned off by slowly lowering the gate voltage Vge, which effectively reduces the di/dt, and then reduces the voltage peak at the turn-off moment. Thus, the short-circuit protection of IGBT is achieved.

In normal operation (e.g. rated current or overcurrent) it is not enabled. Therefore, it is necessary to adapt a suitable turn-off resistor according to the actual operating conditions, or to take appropriate measures to avoid excessive turn-off peaks during normal operation.

The SSD function also has its limitations on the suppression of turn-off peaks, excessive DC bus stray inductance can still lead to large turn-off peaks under short-circuit conditions. Therefore, it is necessary to analyze the short-circuit behaviour of IGBTs in all kinds of extreme operating conditions. Firstack suggests that it is the best to simulate the actual operating conditions for short-circuit testing to ensure that the V_{CE} of IGBT in short-circuit conditions has sufficient safety margins.

Active Clamping

If the V_{CE} voltage peak is too high and cannot be reduced by other means, basic active clamping is recommended.

When the collector-emitter voltage exceeds the preset threshold, the active clamping action is triggered, which partially turns on the IGBT, thus suppressing the collector-emitter voltage of the IGBT, and the IGBT operates in the linear region at this time.

The basic active clamping circuit connects the collector and gate of the IGBT via the transient voltage suppressor (TVS).

The 2FHC0215xV supports the basic active clamping function. The reference circuit is shown in **Fig.12**.

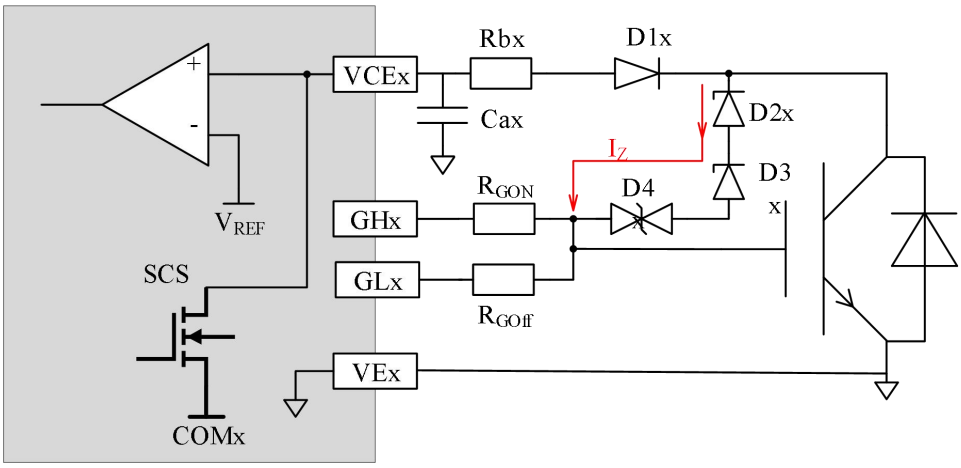


Fig.12 Basic active clamping

TVS D2x, D3x, D4x are connected in series to form an active clamping network, **Fig.12** is only schematic, the number and specifications of the series connection are selected according to the actual operating conditions, and it is recommended to have 3 to 6 of them.

TVS D2x, D3x, D4x are recommended:

VDC-LINK = 800V, the sum of the VR of the TVS is recommended as 780V, e.g. six 130V TVS.

VDC-LINK=1200V, the sum of the VR of the TVS is recommended as 1200V, e.g. six 200V TVS.

At least one or more of them must be a bidirectional TVS (e.g. D4x in **Fig.12**) to avoid positive conduction of the TVS network when the IGBT is turned on in the turn-on state. The TVS breakdown voltage and current will be different between different brands, it is recommended to debug and match according to the actual application.

Please note that when setting the TVS threshold, it is necessary to avoid frequent triggering of the TVS during normal operation. The efficiency of the active clamping is highly dependent on the TVS type (manufacturer), and it is recommended to re-evaluate the test when replacing the TVS to avoid application risk.

The performance of active clamping can be improved by increasing the resistance value of the gate resistor R_{GOFF}.

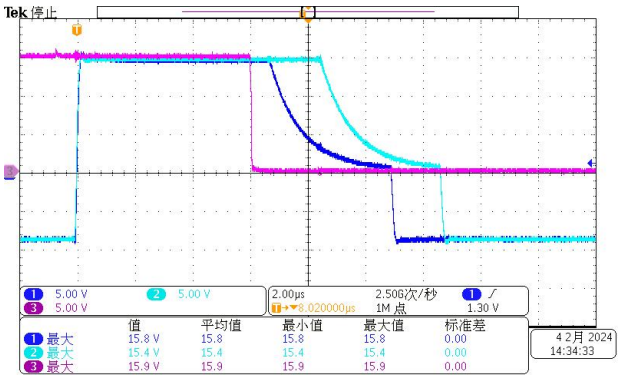
The active clamping function is externally configurable, if not applicable, omitting D2x, D3x and D4x.

3-Level Timing Sequence Management

The turn-off sequence of the inner and outer IGBTs at the moment of fault can effectively protect the IGBT to safely turn off under 3-level application.

At this point, CH1 must be configured as the outer IGBT and CH2 as the inner IGBT.

The digital ASIC chip design enables self-processing of the secondary side communication for fault sequence turn-off.



Inner IGBT(CH2) has a fault, communicates to the outer IGBT(CH1), and both CH1 and CH2 perform timing sequence soft shut down.

Outer IGBT(CH1) has a fault, communicates to the inner IGBT(CH2), and both CH1 and CH2 perform timing sequence soft shut down.

Technical Support

Firstack's professional team will provide you with business consultation, technical support, product selection, price, lead time and other related information, and guarantee to answer your questions within 48 hours.

Legal Disclaimer

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