2FHD0620

Application Manual

SiC gate driver, supports multi-level

The 2FHD0620 is a dual-channel SiC gate driver developed by Firstack for up to 1700V EconoDual module, and can support max. 4 modules in parallel.

The gate driver incorporates advanced features such as active Miller clamping, soft shut down and distributed NTC sampling, which can drive the SiC MOSFET module safely and reliably.

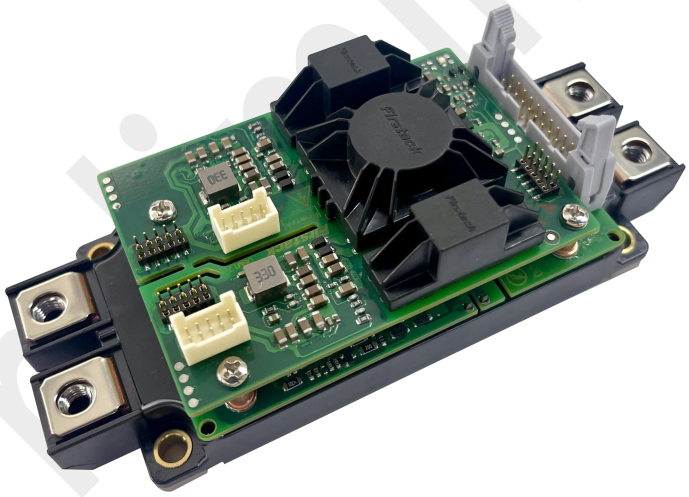


Fig.1 2FHD0620

Contents

Abstract

The 2FHD0620 is a high-performance, dual-channel gate driver developed based on intelligent chip technology by Firstack, supports SiC modules up to 1700V. It features distributed NTC sampling function that leverages Firstack ASIC technology, which can perform the temperature sampling from all modules, capturing a comprehensive temperature information rather than just the peak temperature. The core board and main adaptor board is connected by the connector(pin header), which can be used as a plug-and-play drier. Via a set of customized cables, the sub adaptor board can be connected to core board and drive max. up to four modules in parallel.

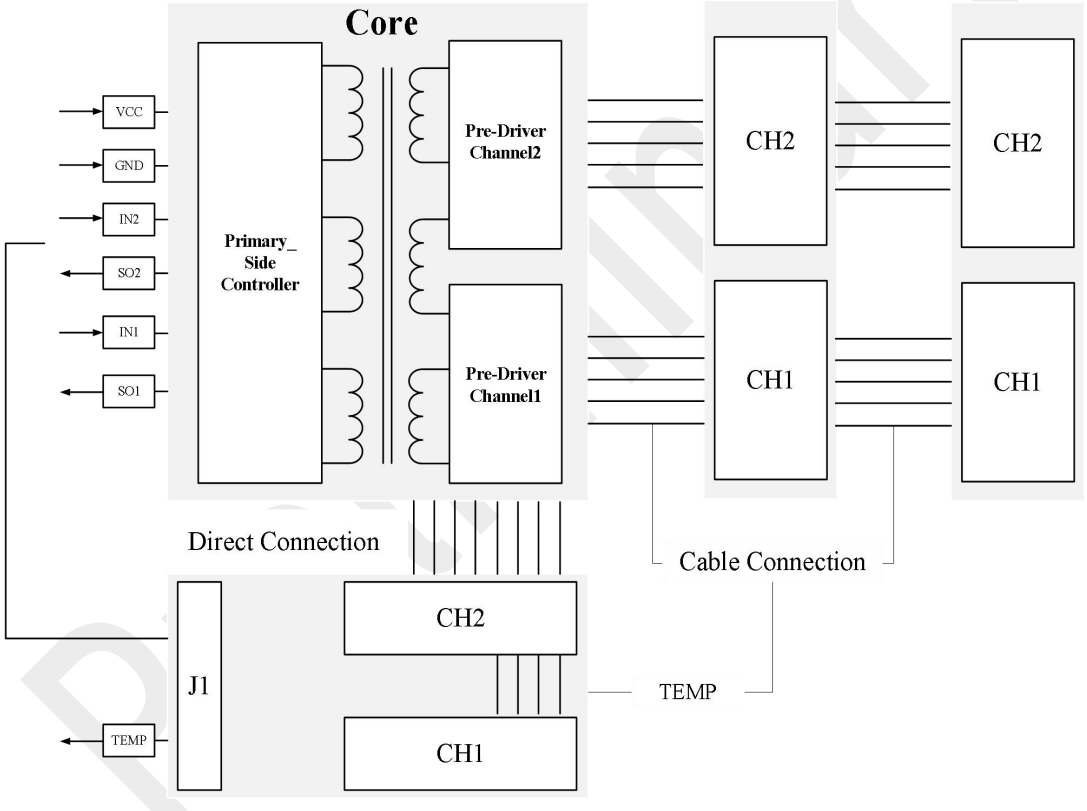


Fig.2 2FHD0620 block diagram

Use steps and safety notice

Simple use steps of the gate driver are as follows:

1. Choose suitable gate driver

When using the gate driver, pay attention to the model of the SiC module that the gate driver is adapted to. It is invalid for non-designated SiC modules. Improper use may cause the gate driver and the module failure.

2. Install the gate driver on the SiC module

Any treatment of SiC modules or gate drivers should follow the general specifications for the protection of electrostatic sensitive devices required by the international standard IEC 60747-1, Chapter IX or IEC 60340-5-2 (which means the workplace, tools, etc. must comply with these standards).

If these specifications are ignored, both the SiC module and the gate driver may be damaged.

3. Connect the gate driver to the control unit

Connect the gate driver connector to the control unit and provide a suitable power supply voltage for the gate driver.

4. Check the function of the gate driver

Check the gate voltage: for the turn-off state, the rated gate voltage is given in the corresponding data sheet, for the turn-on state, the voltage is 15V. Please also check the input current of the gate driver with and without a control signal.

These tests should be performed before installation, because the gate terminal may not be accessible after installation.

5. Set up and test the power unit

Before starting the system, it is recommended to check each SiC module with a single pulse or

double pulse test method. Firstack specially reminds: even under the worst conditions, it is necessary to ensure that the SiC module does not exceed the operating range specified by SOA, because the operating condition of the SiC module strongly depends on the specific converter architecture.

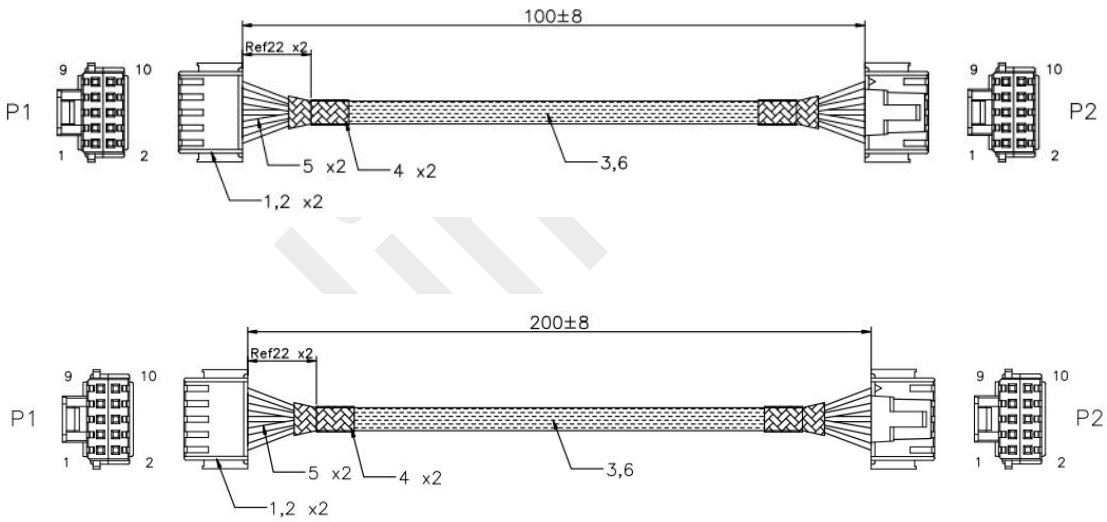
Even when testing a single SiC module, power must be supplied to the other gate drivers in the system to ensure that the gates of all other SiC modules operate in negative voltage turn-off state. This is particularly important when testing the switching behaviour of the SiC module.

Cable Description

With a set of cables 2FHD0620 is enable to be used for paralleling. There is prepared connectors for cables on the core board. Customer only needs to choose the suitable length of cable by actual application.

Note: The cable is special designed for corresponded product, if customer uses their own cables, we can not promise the performance.

Part Number	Cable Length (mm)	Pin Definition
JWDET-00618	200	3rd pin as ground
JWDET-00810	100	



Assemble/Disassemble Description

Three M3 screws are used to mount the core board and adaptor board in order to increase the flexibility of the GDU(gate driver unit) for customer. By removing three M3 screws the core board can be easily disassembled.

Primary Side Characteristics

1. Description of Primary Side Interface

The primary side interface of 2FHD0620 is a 20-pin interface connector on the adaptor board:

- 2x power supply terminals (only 15V is required)
- 2x drive signal inputs
- 2x fault signal outputs
- 10x GND (common ground)
- 1x TEMP
- 3x NC (free)

2. V_{CC}

The 2FHD0620 is equipped two V_{CC} power terminals, which supplies the power to both primary side and isolated DC/DC converter, in order to provide positive and negative voltage to secondary side. The maximum current of the gate driver is 120mA.

3. INx

The signal input pin of the gate driver, supports 5-15V logic level, the matching of resistors is important during design process, 10k pull-down resistor is recommended.

The function of INx is related to the driving mode, which is selected by software(SW), and cannot be adjusted by hardware(HW).

Direct Mode:

IN1 and IN2 are independent signals. CH1 and CH2 can be turned on simultaneously.

Half-bridge topology: To avoid CH1 and CH2 both in high voltage level, which causes the short-circuit, the dead time must be enough set by controller.

Half-bridge Mode:

IN1 is the input terminal of drive signal (PWM), IN2 is the enable terminal (EN);

IN2 is low, two outputs are blocked, all output signals are low.

IN2 is high, two outputs are enabled, output signals are changed follow the changing of IN1.

When IN2 is high, IN1 converts from high to low, the gate signal of CH2 is blocked immediately and turns on after dead time T_d.

Attention: The default dead time T_d is 4μs, which is set through software, can not be changed from outside circuit. When IN2 increases to high, the output will change follow the changing of IN1 after dead time.

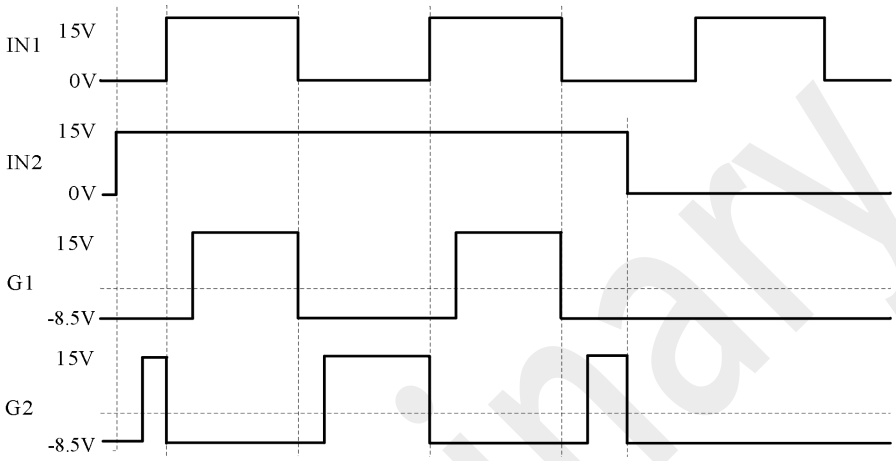


Fig.3 Logic diagram of half-bridge mode

4. SO1, SO2 Status Output

The outputs SOx have open-drain transistors, which is by default a single fault signal to locate the failure precisely. They can also be connected together to provide common fault signal.

Under fault status, the current flowing through SOx can not exceeds 10mA defined in the data sheet.

When there is no fault, the output is high, the pull-up resistor is required on main control board. The recommended range of pull-up voltage is 5-15V, resistor value: 5V---3.3K-4.7K, 15V---10K -15K.

When channel “x” detects fault, SOx will be low (connected to GND).

SOx Output Logic

When an undervoltage occurs in primary side, GDU will be turned off directly negatively and keep blocking for a blocking time, at the same time both of SOx goes to high after report 40ms low level fault.

If the undervoltage disappears before this process, SOx will keep high. If the undervoltage still occurs, the fault will be pulled down again until the fault disappears, then return to high after a blocking time (80ms).

Primary side blocking signal: After the primary side undervoltage fault disappears, after another 80ms the blocking is over, primary side process the INx signal normally.

When an undervoltage occurs in secondary side of the gate driver, gate performs soft shut down first. After the off status in negative voltage for a defined time, the signal will be blocked in 0V, the corresponding SOx signal reports 20ms low level fault and after that returns to high level 100ms.

If the undervoltage disappears before the above process, SOx keep high; If the fault still occurs, the signal will be pulled down again until the fault disappears, then after another 80ms the SOx signal returns to high level.

Primary side blocking signal: After the secondary side undervoltage fault disappears, then after 60-80ms the blocking is over, primary side process the INx signal normally.

When a short-circuit fault occurs on the secondary side of the driver, the gate first performs the soft shutdown function, then puts in a negative voltage to keep the shutdown state and maintains the blocked signal, the corresponding SOx signal reports the fault, and then automatically restores the high level after pulling it down for 10ms.

The 2FHD0620 is equipped with Intelligent Fault Management, please refer to Intelligent Fault Management for T_{SOX} details.

5. TEMP

The pin which is used for the distributed NTC sampling, totally three different output choices: UART (all temperature from all modules), Frequency or Duty Cycle.

Secondary Side Characteristics

1. Description of Secondary Side Interface

A 10-pin interface is equipped on both channels on the core board as J2 and J3. An extra pin in CH1 is used for the distributed NTC sampling.

- 1x Secondary side ground terminal V_{EE}
- 3x Secondary side negative terminal V_{SS} (CH2)
- 2x Secondary side negative terminal V_{SS} (CH1)
- 1x Secondary side positive terminal V_{DD}
- 1x 5V Power
- 1x TC signal
- 1x Active miller clamping signal (AMC)
- 1x Soft shut down signal (SSD)
- 1x Gate signal
- 1x NTC_Tx / NTC_Rx (CH1)

2. Secondary Side Ground Terminal V_{EE}

The V_{EE} terminal provides the reference ground for the secondary side.

3. Secondary Side Negative Terminal V_{SS}

The negative terminals Vss provide negative voltage for the secondary side, the rang of negative voltage is around -9 to -0.5, which is related to the secondary side positive voltage V_{DD} and HW.

4. Secondary Side Positive Terminal V_{DD}

Positive voltage of secondary side, which is decided by the SW.

5. 5V Power

5V power is used to power the digital isolator.

6. TC Terminal

The 2FHD0620 is enable to detect the short-circuit during the operation of SiC module and start

soft shut down to turn off the module safely by Desaturaion Detection. There are two detection methods: Resistor Detection and Diode Detection. Diode detection is initialized for the 2FHD0620 .

Diode Detection

The diode detection circuit can achieve high accuracy and fast reaction to protect the module during short circuit situation.

During the normal operation time the current will flow through the low impedance circuit consisting of diodes and a resistor, which is used to limit the current. When the short-circuit occurs, the V_{ds} will increase due to the desaturation of the module, which will cause the reverse cut off of the diode, so that the current won't flow through the diode anymore and start charging the capacitor. When the voltage exceeds the threshold V_{ref}, the TC signal will be activated and SSD signal will convert from low to high to start soft shut down function.

The short-circuit detection time is around 1.2μs.

7. Active Miller Clamping (AMC)

The AMC is used to pull down the gate voltage to a certain negative voltage to avoid the mistaken turn-on. Especially the high turn on speed of SiC MOSFET will cause gate coupling and lead to the short-circuit due to the mistaken turn on of the MOSFET.

The AMC signal comes from the ASIC by Firstack. During the turn-on process the AMC signal will be low and after the filter time 1μs in the turn-off process the signal will convert to high to activate the miller clamping.

8. Soft Shut Down (SSD)

When the short-circuit is detected, the gate signal will be in high impedance and SSD signal will turn on the MOS, so that the current will flow through the SSD resistor, which is 10 - 20Ω and depends on the modules. In another word, SSD function achieve the change of turn-off resistors during the short circuit situation.

The SSD function also has its limitations on the suppression of turn-off peaks, excessive DC bus stray inductance can still lead to large turn-off peaks under short-circuit conditions. Therefore, it is

necessary to analyse the short-circuit behaviour of SiC MOSFET in all kinds of extreme operating conditions. Firstack suggests that it is the best to simulate the actual operating conditions for short-circuit test to ensure that the V_{DS} of SiC MOSFET in short-circuit conditions has sufficient safety margins.

If the V_{DS} voltage peak is too high and cannot be reduced by other means, the basic active clamping function is recommended.

9. NTC_Tx / NTC_Rx

Normally GDU can detect the highest temperature and report it to the master computer. However sometimes the complete temperature information is also important for customer to observe the operation status and optimize the architecture for heat dissipation. Therefore Firstack develops NTC sampling circuit continuously, which named as Distributed NTC (DNTC). **Fig.4** introduces the basic topology. There are several advantages of this new design:

1. Temperature sampling from all modules
2. Communication between all GDUs based on the bus protocol
3. High robustness and precision temperature information
4. Uniform design for all kinds of modules

The NTC will sample from the first adaptor board to the core board or the last adaptor board. During the transport process, the temperature information will be saved and transported in sequence to the next microcontroller. Finally the last microcontroller will transmit all temperature or the highest temperature based on the choice of the SW to the master computer.

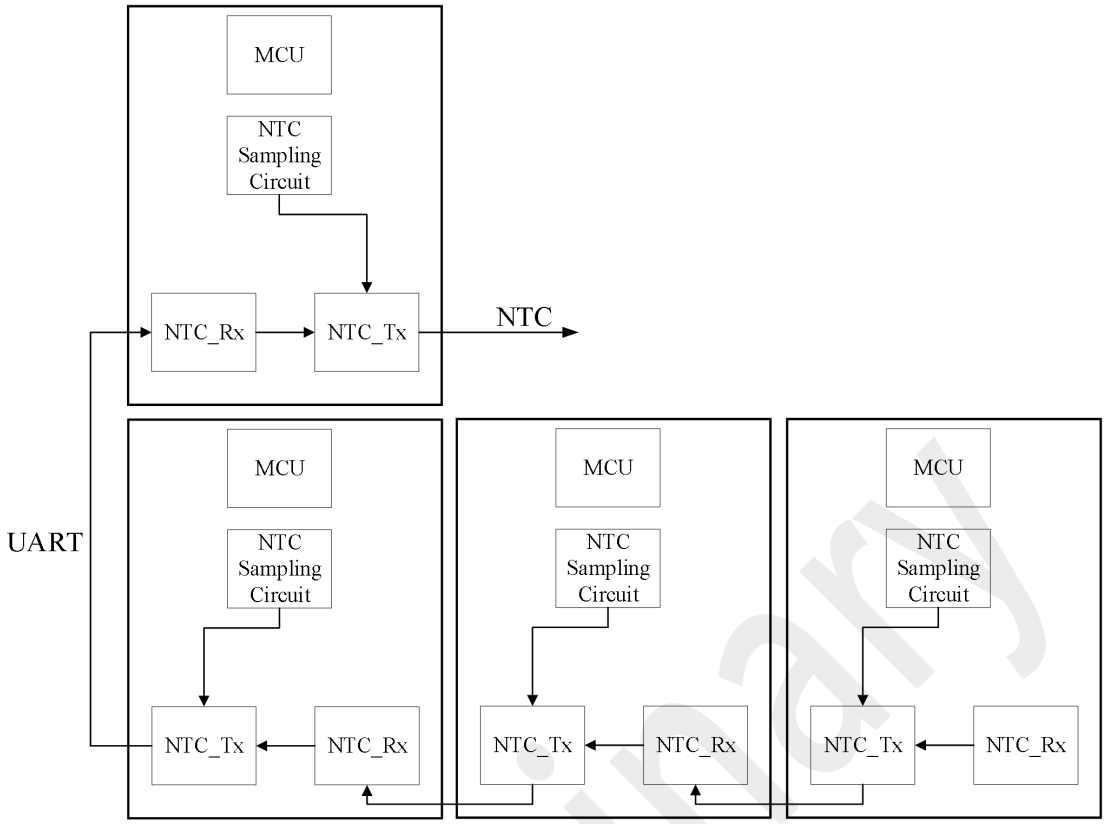


Fig.4 Distributed NTC sampling circuit topology

Technical Principle

1. Power Supply and Electrical Isolation

The gate driver implements isolated power and signal. Power isolation is realized by the transformer, signal isolation is realized by capacitive coupling. The transformer complies with the safety isolation standard EN50178 and the primary and secondary sides fulfil protection class 2.

Please note that a stable supply voltage and current are required to power the driver.

2. Power Monitoring

The primary side of the driver, as well as the two secondary side power supplies, have local power detection circuits, as well as corresponding undervoltage protection.

When undervoltage occurs in the primary power supply, both channels are driven by the negative gate voltage to maintain the shutdown state (both channels are blocked), and both SO1 and SO2 feed back the fault status signal to the master computer.

When the positive or negative voltage on the secondary side is lower than the threshold voltage, the driver circuit will determine that an undervoltage fault has occurred, and the driver circuit will automatically block the MOSFET, and at the same time, the corresponding -SOx will feedback a fault signal to the master computer.

The SOx outputs are automatically reset after the primary and secondary undervoltage faults are removed.

Firstack recommends against operating either IGBT in the bridge arm in an undervoltage state.

Due to the presence of C_{CG}, when one IGBT in the bridge arm turns on, the high dv/dt from it can be coupled to the other IGBT through the C_{CG}, resulting in micro-conduction of the other IGBT.

3. Intelligent Fault Management

The driver detects the operation status of the module in real time, and when the module fails, it uploads the fault status to the master computer through the SOx output, and the 2FHD0620 realizes the fault differentiation by the difference of the pull-down time of the SOx signal (the

fault return time).

For more information, see the table below.

Fault Type	Short-circuit	Undervoltage(sec.)	Undervoltage(pri.)	Other Faults
Return time (Tsox)	10ms	20ms	40ms	80ms

Technical Support

Firstack's professional team will provide you with business consultation, technical support, product selection, price, lead time and other related information, and guarantee to answer your questions within 48 hours.

Legal Disclaimer

This manual gives a detailed introduction about the product, but cannot promise to provide specific parameters. No warranty or guarantee, express or implied, is given herein as to the delivery, performance or applicability of the product.

Firstack reserves the right to modify technical data and product specifications at any time without prior notice. Firstack's general payment terms and conditions apply.

Company Information

Tel: +86-571 8817 2737

Fax: +86-571 8817 3973

Web: www.firstack.com

Email: fsales@firstack.com

Address: 4-5/F, Building/5, Xizi Wisdom Park, No.1279 Tongxie Road, Hangzhou, China