2FHC0215

Application Manual

Compact gate driver core, supports multi-level

The 2FHC0215 is a dual-channel gate driver with electrical interface. It is also with ASIC digital control for safe and reliable driving of IGBT. The gate driver is suitable for all common IGBT up to 900A/1700V and supports multi-level topology.

The 2FHC0215 is a compact driver core with dimensions of 45mm*34mm and a maximum height of 15mm.

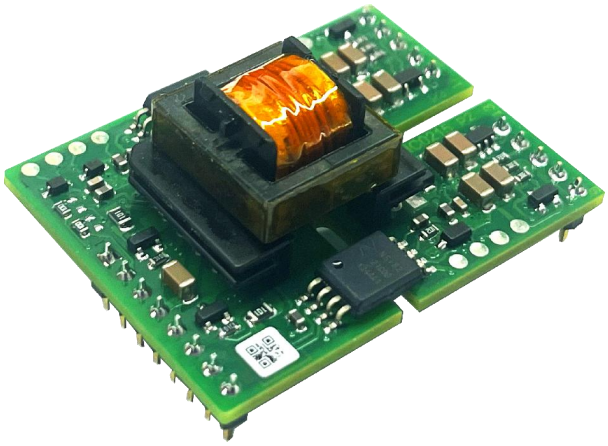

Fig.1 2FHC0215

Contents

Driver Overview

The 2FHC0215 is a compact gate driver core developed by Firstack based on digital control, the target market is the low to medium power, dual-channel IGBT applications such as general purpose inverters, UPS, power quality, and so on.

The 2FHC0215 contains a complete dual-channel IGBT driver core with isolated DC/DC converter, short-circuit protection and supply voltage monitoring with SSD, intelligent fault management.

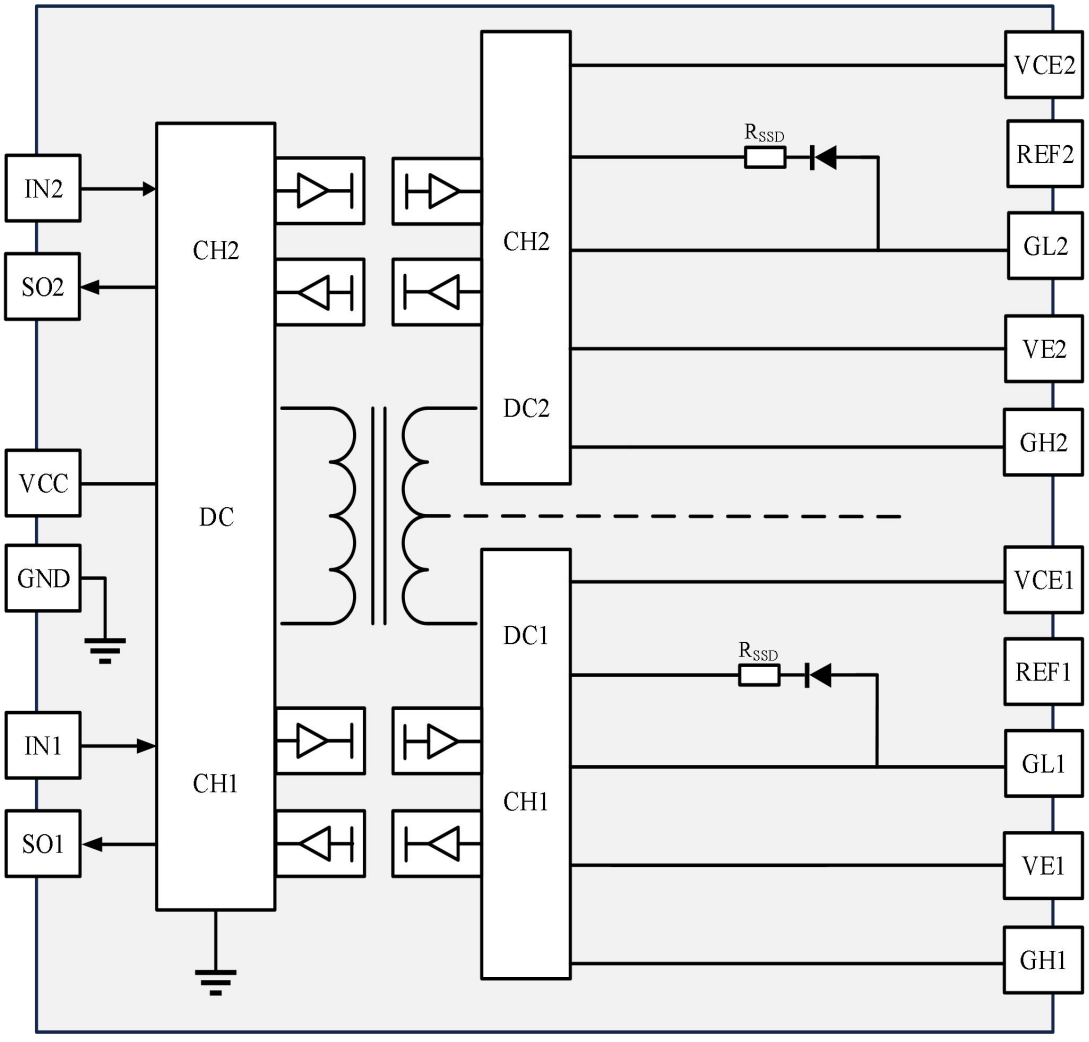

Fig.2 2FHC0215 block diagram

Pin Designation

Pin	Definition	Function
Primary Side		
1	GND	Ground
2	IN1	Input channel 1, as control signal in half bridge mode
3	IN2	Input channel 2, as enable signal in half bridge mode
4	VCC	15V supply voltage for primary side
5	NC	Free
6	SO2	Fault signal channel 2; normal high-impedance, 0V on fault
7	SO1	Fault signal channel 1; normal high-impedance, 0V on fault
8	NC	Free
Secondary Side		
9	GH1	Gate high channel 1
10	VE1	Emitter channel 1 (ground)
11	GL1	Gate low channel 1
12	REF1	Set V_{CE} detection threshold channel 1
13	VCE1	V_{CE} sense channel 1
14	Free	
15	Free	
16	Free	
17	GH2	Gate high channel 2
18	VE2	Emitter channel 2 (ground)
19	GL2	Gate low channel 1
20	REF2	Set V_{CE} detection threshold channel 2
21	VCE2	V_{CE} sense channel 2

Primary Side Characteristics

Recommended Interface Circuit for Primary Side

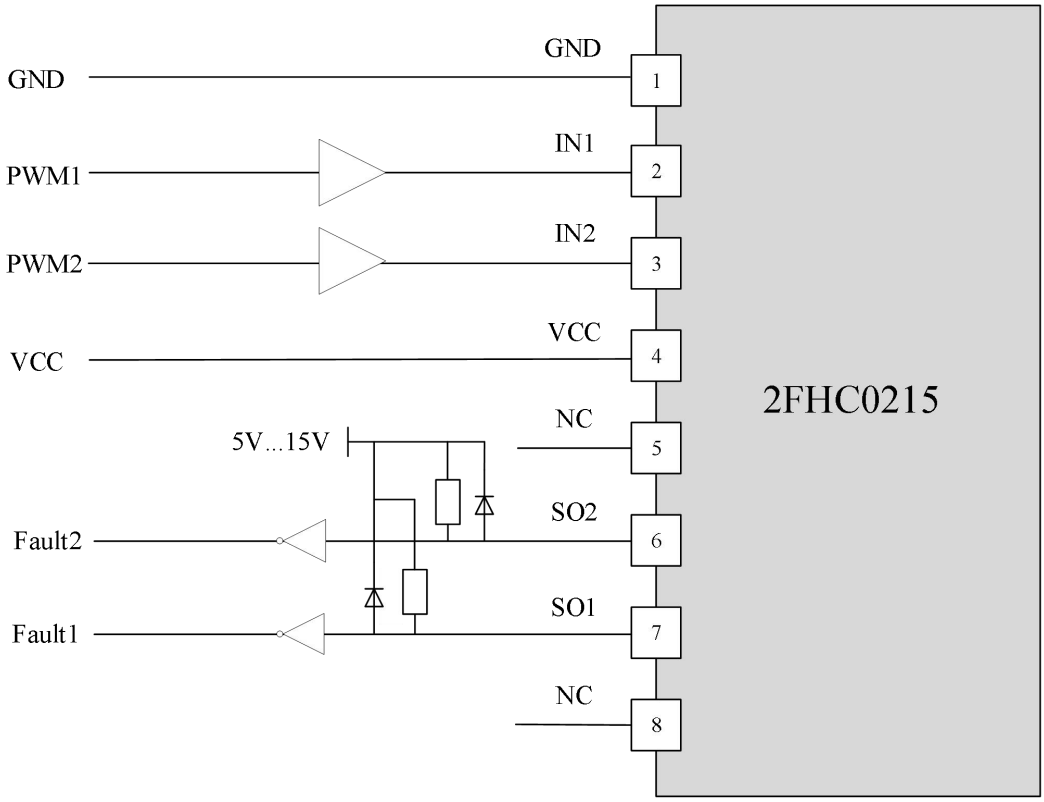

Fig.3 Recommended user interface of 2FHC0215 (primary side)

Description of Primary Side Interface

The primary side interface of 2FHC0215 is quite simple and easy to use.

Primary side is equipped with an 8-pin interface connector:

- 1× power supply (only 15V is required)
- 2× drive signal inputs
- 2× fault signal outputs
- 1× GND (ground)
- 2× NC (free)

V_{CC}

The 2FHC0215 is equipped with a V_{CC} power terminal to supply power to both primary side circuit and isolated DC/DC converter and provide positive and negative voltage to the secondary

side. The maximum current of the gate driver is 450mA.

INx

The signal input pin of the gate driver, supports 5-15V logic voltage, the resistance matching is important during design process, 33K-68K pull-down resistors are recommended.

The function of INx is related to the gate driver mode, which is set by software, and cannot be adjusted by external hardware.

Direct Mode：

IN1 and IN2 are independent. CH1 and CH2 can be turned on simultaneously.

Half bridge topology: To avoid a short-circuit caused by CH1 and CH2 being high at the same time, the control circuit must be set with sufficient dead time.

Half bridge Mode：

IN1 is the input terminal of drive signal (PWM), IN2 is the enable terminal of signal (EN);

If IN2 is low level, two outputs are blocked, all output signals are low level.

If IN2 is high level, two outputs are enabled, output signals are changing with IN1.

When IN2 is high level, IN1 turns from low to high, the gate signal of CH2 is blocked immediately, CH1 gate is turned on after dead time T_d.

Attention: The default dead time T_d is 4μs, which is set by software and can not be changed by hardware. When IN2 turns from low to high level, it needs to go through one dead time before the output changes with IN1.

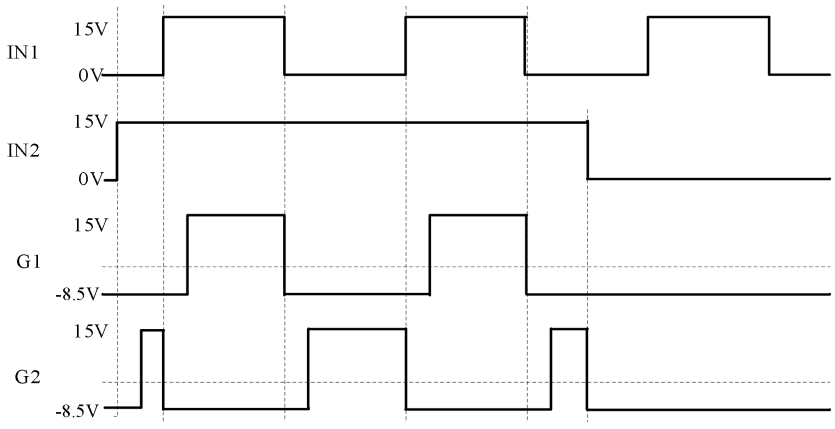

Fig.4 Logic diagram of half bridge mode

SO1, SO2 Status Output

The outputs SOx have open-drain transistors, which is by default a single fault signal to point the problem precisely. They can also be connected together to provide common fault signal.

Under fault condition, the current flowing through SOx can not exceeds 10mA defined in the data sheet.

When there is no fault, the output is high, the pull-up resistor is required to install in main control board. The recommended range of pull-up voltage is 5-15V, resistor value: 5V---3.3K-4.7K, 15V---10K-15K

When channel “x” detects fault, SOx will be low (connect to GND).

SOx Output Logic

When an undervoltage occurs on primary side of the driver, gate will be turned off directly with negative voltage and keep blocking for a blocking time, at the same time both of SOx goes to high after reporting 40ms low level fault.

If the undervoltage disappears before this process, SOx will keep high. If the undervoltage still exists, the fault will be pulled down again until it disappears, then return to high after a blocking time (80ms)

Primary side blocking signal: After the primary side undervoltage disappears, then after 80ms the blocking is over, primary side processes the INx signal normally.

When undervoltage occurs on secondary side of the gate driver, gate performs soft shut down first. When the negative voltage continues for a while, keep 0V turn-off and maintain blocking signal, the corresponding SOx signal reports 20ms low level fault and after that returns to high level for 100ms.

If the undervoltage disappears before the above process, SOx keep high; if the fault still exists, the fault signal will be pulled down again until the fault disappears, then after 80ms the SOx signal returns to high level.

Primary side blocking signal: After the secondary side undervoltage disappears, then after 60-80ms the blocking is over, primary side processes the INx signal normally.

When a short-circuit occurs on the secondary side of the gate driver, the gate first performs the soft shut down, then puts in a negative voltage to keep the shutdown state and maintains blocking signal, the corresponding SOx reports the fault, and then automatically restores the high level after pulling down for 10ms.

The 2FHC0215 is equipped with intelligent fault management, for T_{SOX} details please refer to Intelligent Fault Management.

Secondary Side Characteristics

Recommended Interface Circuitry for Secondary Side Connector

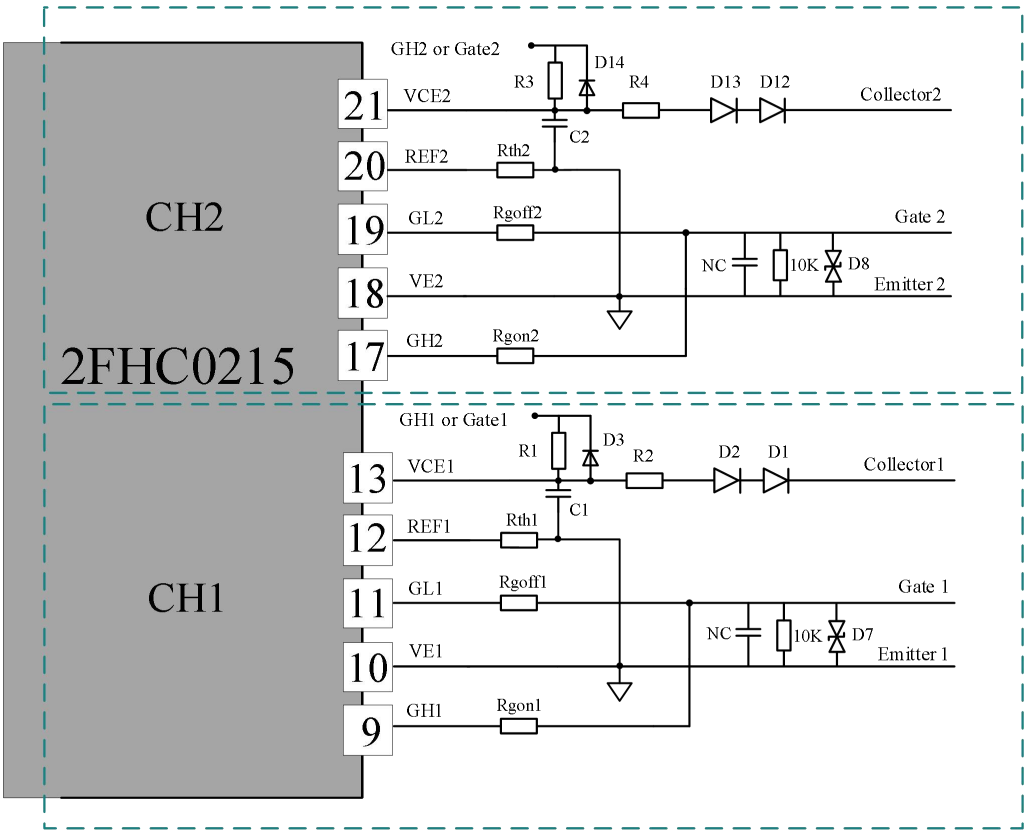

Fig.5 Recommended circuit for secondary side

Description Secondary Side Interface

The secondary side has two channels with a 5-pin interface terminal respectively:

- 1× emitter VEx
- 1× reference REFx (for shot-circuit protection)
- 1× VCEx
- 1× gate turn-on GHx
- 1× gate turn-off GLx

Emitter Terminal VEx

The emitter terminal must be connected to the auxiliary emitter of the IGBT according to the circuit in **Fig. 5**.

Reference Terminal (REFx)

This pin of the gate driver is internally connected to a 33k resistor pull-up to VISOx, and a Rthx is connected between REFx and VEx for setting the short-circuit detection voltage threshold.

VREFx voltage calculation formula is:

$$\mathrm{VREFx} = \mathrm{VISOx} * \frac{\mathrm{Rthx}}{33\mathrm{k} + \mathrm{Rthx}}$$

It is recommended to connect a 68k resistor between REFx and VEx, at which point the VREFx value is 10.1V. This part of the circuit should be located as close as possible to the gate driver pins to reduce the amount of parasitic inductance, and it is recommended to increase the Cthx capacitance by 10-47pF to increase the immunity to interference of VREFx.

Collector Electric Potential Detection Terminal (VCEx)

The 2FHC0215 collector potential detection supports both resistor detection and diode detection. It needs to be connected to the collector of the IGBT according to the corresponding recommended circuit to detect the short circuit of the IGBT.

1) Resistor Detection

The reference resistor detection circuit is like:

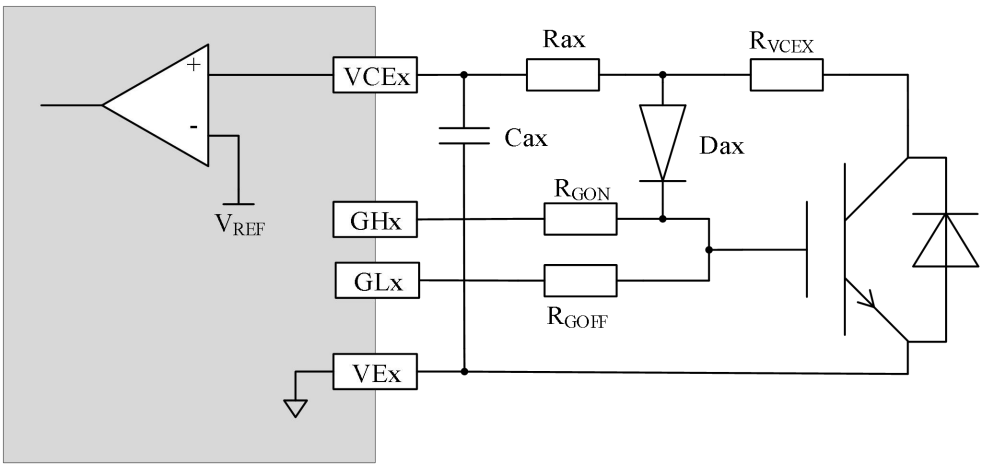

Fig.6 Resistor detection reference circuit

When the IGBT turns off, the gate driver internally pulls the VCEx potential to the COMx potential (negative supply voltage). At this time, capacitor Cax discharges to the negative supply voltage, which is about -8 V with respect to VEx. During this time, the current flows into the gate

GLx through the resistor network RVCEX and the diode Dax. The resistor network acts as a current limiter. The position of Dax in the above figure can be connected to both ends of RGON, as shown in the above figure on the left side of the power supply without resistor RGON differential voltage.

RVCEX resistance range is recommended so that the current flowing through the resistor IRVCEX = 0.6~1mA, (e.g., 1200V bus voltage, the recommended resistance value is 1.2~2MΩ), the maximum does not exceed 1mA. High voltage resistors or multiple resistors in series can be used. When designing the peripheral circuit, attention must be paid to the minimum creepage distance.

During the turn-on process and conduction state of the IGBT, GHx turns on, GLx turns off, the gate voltage is +15V, and Dax cuts off. As the VCE voltage decreases, the Cax potential is charged from COMx to the IGBT saturation voltage drop. The bus voltage charges Cax through RVCEX and Rax and the charging time is determined by the bus voltage, Rax and Cax.

For 600V IGBT, it is recommended that Rax=62kΩ, for 1200V~1700V IGBT, it is recommended that Rax=120K.

The response time of 2FHC0215 consists of SCS time(software fade time, about 3us), Cax charging time, SC filtering time(Tsc_filter time, short for Tsc_ft, set as 1us).

The SCS time is the time from the turn-on of the IGBT to the internal chip of the gate driver detects a short-circuit fault. Cax charging time is the time from the turn-on of the gate to the time when the VCEx voltage reaches the VCE monitoring threshold. SC filtering time is the time from the time when the VCEx voltage exceeds the VCE monitoring threshold to the time when the gate driver determines that a short-circuit fault has occurred.

The relationship between the three is as follows: when SCS time > Cax charging time, the response time is equal to SCS time + SC filter time; when SCS time < Cax charging time, the response time is equal to Cax charging time + SC filter time. The SCS time and SC filter time are set by the programme, and the SCS time + SC filter time ≈ 4us.

The following table lists the response time Tax corresponding to different Cax values to make it easier to set the desired response time.

For applications with busbar voltage VDC>550V, RVCEX=1.8MΩ, Rax=120kΩ is recommended.

Cax (pF)	Rthx (kΩ)	Tax (μs)
0	68	4
15	68	5.9
22	68	7
33	68	8.9
47	68	11.8

When the DC bus VDC is <550V (Rax=120kΩ), the response time rises.

Since the presence of parasitic capacitance in practice may affect the response time, it is recommended that actual measurements be made in the final design. When defining the response time, it is important to ensure that it is less than the maximum short-circuit duration allowed by the power semiconductor used.

Diode Dax must have a very low leakage current, a blocking voltage must be more than 40 V and no Schottky diodes can be used. Components Cax, Rax, Dax must be positioned as close to the driver as possible. Avoid large collector-emitter loops.

When a short-circuit/over-current fault is detected, the driver switches off the responding power semiconductor. The fault state is immediately transmitted to the corresponding SOx output. After a blocking time Tb, the driver resumes processing the input signal.

2) Diode Detection

The diode detection circuit can adapt to the low V_{CE} voltage, for the 2FHC0215 it is recommended to use the diode detection circuit.

When the IGBT is turned off, the internal circuit of the gate driver pulls the VCEx pin voltage down to the COMx potential, at which point capacitor Cax discharges to the negative supply voltage, which is about -8V with respect to VEx.

During the turn-on process and conduction state of the IGBT, GHx turns on, GLx turns off, the gate voltage is +15V, D2x cuts off, the capacitor Cax is charged through Rax, and the voltage of Cax rises. When the collector voltage of the IGBT decreases to a certain potential, the voltage of Cax is clamped by the high voltage diode D1x.

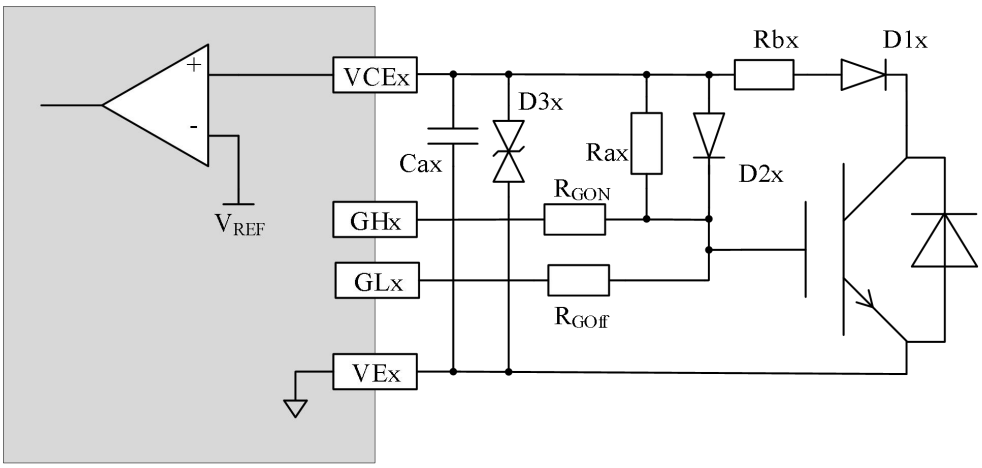

Fig.7 Diode detection reference circuit

As shown in **Fig.7**, the voltage across Cax is calculated as follows:

$$VCax = VCEsat+VF(D1x)+Rbx*\frac{15V-V_{CEsat}-V_{F(D1x)}}{Rax+Rbx}$$

The value of the SC detection threshold voltage VREF must be higher than Vcax, and the default VREF value for the 2FHC0215 is 10.1V.

Rax and Cax can be used to set the response time Tax required for turn-on according to the following formula:

$$Rax[k\Omega] = \frac{T_{ax}[us]-Tsc\_ft}{Cax[pF]*ln(\frac{15V+|VGLx|}{15V-Vrefx})}$$

Recommended circuit component parameters are as follows：

- D1x: 2 US1M used for 1200V IGBT
  2-3 US1M used for 1700V IGBT
- D2x: Fast diodes, such as the BAS316, require low leakage currents and cannot use Schottky.
- D3x: 15 V transient voltage suppression diode TVS, can also be omitted
- Rax: 5kΩ~10kΩ, it is recommended to connect more than two 1206 resistors with the same power in parallel.
- Rbx: 100Ω~330Ω
- Cax: 100pF~1000pF

Cax needs to take into account the suppression diode D3x and the PCB parasitic capacitance.

Note: When the react time Tax≤4μs, Tax=4μs.

When the react time Tax> 4μs, Tax is equal setting value.

3) Shield V_{CE} sense

Emulating V_{CE} sense and shielding are required to operate the gate driver without the IGBT module for testing and evaluating the driver function under weak power.

For the resistor detection circuit, if give the gate driver a turn-on signal without connecting the module, the driver gate will automatically respond; emulating short-circuit detection function can be achieved by shorting the D2x diode, it should be noted that the short-circuit response time under the weak power is slightly larger than the actual value of the circuit design (the actual value needs to be measured in the strong power test platform with the CE terminal provided with the bus voltage).

For the diode detection circuit, if give the gate driver a turn-on signal without connecting the module, the gate driver will automatically detect a short-circuit fault, and if the short-circuit response time is unstable, please apply a 15V voltage between the collector and the emitter; shielding the short-circuit detection function requires the formation of a low impedance between the collector and the emitter to simulate the IGBT conduction state, or you can short the them, but at this time, it is not permitted to supply power to the CE terminal. .

Gate Drive Terminal (GHx & GLx)

The gate driver connects resistors to the gates of the IGBTs through the gate drive terminals. The GHx and GLx pins control the turn-on and turn-off of the IGBTs respectively, and the turn-on and turn-off resistors can be set separately as required. The design can be made with reference to **Fig. 5**.

It is recommended to connect a 10k to 22k resistor between GLx and VEx. This resistor can provide a low impedance loop between the IGBT gate and emitter in case of driver power down. Avoid floating voltage causing IGBT false turn-on.

Under IGBT short-circuit conditions, if the VGE voltage is too high, resulting in excessive short-circuit current, a transient voltage suppressor D7 (D8) is connected between the gate and the emitter.

Please note that in half bridge circuits, it is recommended not to generate waveforms for switching

action on the IGBTs with a low supply voltage to the gate driver, otherwise too high rate of change of VCE may lead to partial conduction of the IGBTs.

Technical Principle

Power Supply and Electrical Isolation

This gate driver implements isolated power and signal. Power isolation is realized by the transformer, signal isolation is realized by capacitive coupling. The transformer complies with the safety isolation standard EN50178 and the primary and secondary sides fulfil protection class 2.

Please note that a stable supply voltage and current are required to power the gate driver.

Power Monitoring

The primary side of the driver, as well as the two secondary side power supplies, have local power detection circuits, as well as corresponding UVLO.

When undervoltage occurs on the the primary side power supply, both IGBTs are driven by the negative gate voltage to maintain the turn-off state (both channels are blocked), and both SO1 and SO2 feed back the fault status signal to the master computer.

When the positive or negative voltage of the secondary side is lower than the threshold voltage, the drive circuit will determine that an undervoltage has occurred, and automatically block the IGBT. At the same time, the corresponding SOx will feedback a fault signal to the master computer.

The SOx outputs are automatically reset after the primary and secondary undervoltage faults removed.

Firstack recommends that any IGBT in the bridge arm should not operate in an undervoltage state.

Due to the presence of C_{CG}, when one IGBT in the bridge arm turns on, the high dv/dt from it can be coupled to the other IGBT through the C_{CG}, resulting in micro-conduction of the other IGBT.

Soft Shut Down (SSD)

The full range of 2FHC0215 drives are configured with SSD function.

When the IGBT desaturation occurs, VCE reaches the bus voltage. At the same time, the IC will reach 4 times of the rated current or even more and the di/dt at the turn-off time will form a very

high voltage spike on the parasitic inductance, which will easily damage the IGBT.

When the IGBT desaturation is triggered, the digital core will detect and trigger soft shut down to turn off the IGBT. Within 10us, the IGBT is gradually turned off by slowly lowering the gate voltage Vge, which effectively reduces the di/dt, and then reduces the voltage spike at the turn-off moment. Thus, the short-circuit protection of IGBT is achieved.

In normal operation (e.g. rated current or overcurrent) it is not enabled. Therefore, it is necessary to adapt a suitable turn-off resistor according to the actual working conditions, or to take appropriate measures to avoid excessive turn-off spikes during normal operation.

The SSD function also has its limitations on the suppression of turn-off spikes, excessive DC bus stray inductance can still lead to large turn-off spikes under short-circuit conditions. Therefore, it is necessary to analyze the short-circuit behaviour of IGBTs in all kinds of extreme operating conditions. Firstack suggests that it is the best to simulate the actual operating conditions for short-circuit testing to ensure that the VCE of IGBTs in short-circuit conditions has sufficient safety margins.

Active Clamping

If the peak VCE voltage is too high and cannot be reduced by other means, Firstack recommends to adopt the basic active clamping function.

The active clamping function triggers the active clamping action when the collector-emitter voltage exceeds the preset threshold, which partially turns on the IGBT, thus suppressing the collector-emitter voltage of it, and the IGBT operates in the linear region at this time.

The basic active clamping circuit connects the collector and gate of the IGBT via a transient suppression diode (TVS).

The 2FHC0215 supports the basic active clamping function. The reference circuit is shown in **Fig. 8**.

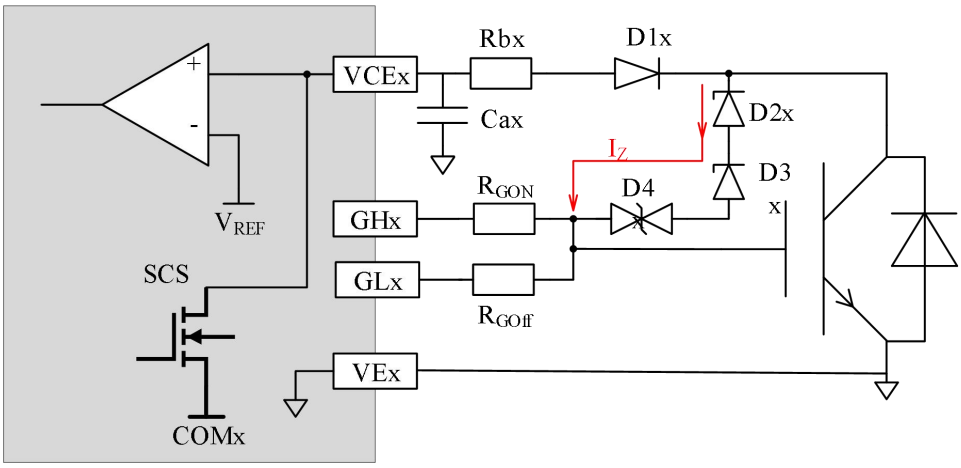

Fig.8 Basic active clamping

TVS diodes D2x, D3x, D4x are connected in series to form an active clamping network, the figure is only schematic, the number and specifications of the series connection are selected according to the actual operating conditions, and it is recommended to have 3 to 6 of them.

TVS D2x, D3x, D4x are recommended:

1) 2-level:

VDC-LINK = 800V, the sum of the VR of the TVS is recommended as 780V, e.g. 6 130V TVS.

VDC-LINK = 1200V, the sum of the VR of the TVS is recommended as 1200V, e.g. 6 200V TVS.

2) 3-level:

VDC-LINK = 1500V, it is recommended that the sum of the VR of the TVS is 1200V, e.g.: 6 TVS of 200V.

At least one or more of them must be a bidirectional TVS (e.g. D4x in **Fig.8**) to avoid positive conduction of the TVS network when the IGBT is turned on in the turn-on state. The TVS breakdown voltage and current will be different between different brands, it is recommended to debug and match according to the actual application.

Please note that when setting the TVS threshold, it is necessary to avoid frequent triggering of the TVS during normal operation. The efficiency of the active clamping is highly dependent on the TVS type (manufacturer), and it is recommended to re-evaluate the test when replacing the TVS to avoid application risk.

Active clamping performance can be improved by increasing the resistance value of the gate resistor RGOFF.

The active clamping function is externally configurable, if not applicable, omitting D2x, D3x, and D4x.

Intelligent Fault Management

The driver detects the operation status of the module in real time, and when the module fails, it uploads the fault status to the master computer through the SOx output, and the 2FHC0215 realizes the fault differentiation by the difference of the pull-down time of the SOx signal (the fault return time).

For more information, see the table below.

Fault Type	Short-circuit	Undervoltage(Sec.)	Undervoltage(Pri.)	Other Fault
Return time(Tsox)	10ms	20ms	40ms	80ms

Technical Support

Firstack's professional team will provide you with business consultation, technical support, product selection, price, lead time and other related information, and guarantee to answer your questions within 48 hours.

Legal Disclaimer

The instruction manual provides a detailed description of the product but does not commit to providing specific parameters regarding the delivery, performance, or applicability of the product. This document does not offer any express or implied warranties or guarantees.

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